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Measurement of Transistor Collector-Emitter Saturation Voltage

K. O. Leedy

Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
Washington, D.C. 20234

June 1977

Final

Prepared for
Defense Nuclear Agency
Washington, D.C. 20305

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U.S. DEPARTMENT OF COMMERCE, Juanita M. Kreps, *Secretary*
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Measurement of Transistor Collector-Emitter Saturation Voltage

K. O. Leedy
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ABSTRACT

This report presents a detailed method for the measurement of collector-emitter saturation voltage. The method which is included in the Appendix is proposed for standardization. The report also contains a description of the laboratory confirmation of the method and a discussion of the precautions to be taken to assure repeatability of the measurement. Emphasized is the necessity to determine that the conditions for saturation are met during the measurement.

INTRODUCTION

There are three regions of transistor operation: cut-off, active, and saturation. These are illustrated in figure 1 which shows curves of collector current versus collector-emitter voltage for different values of base current. For transistors used in switching applications the cut-off and saturation regions are most important. In saturation, or in the "on" state, an ideal transistor switch should have a very low resistance, approaching that of a short circuit so that the voltage drop across the collector-emitter terminals approaches zero. This voltage drop is called the collector-emitter saturation voltage and is usually represented in specification literature by the symbol $V_{CE(SAT)}$.

The saturation voltage is an important parameter because it can be used to predict the performance of a transistor used in switching apparatus such as in d-c to a-c power inverters, chopping circuits, or logic circuits. It represents the "zero" logic level in many types of digital circuits. It is important to know how low the collector-emitter voltage becomes in saturation because during saturation the transistor passes the most current for the longest periods of time, and power dissipation at the collector can become excessive. When a system design is to be used in a radiation environment, it is important to know the change in saturation voltage as a result of radiation dose so that the design can accommodate the changed value.

In the application of a transistor in circuit, it is not always necessary to know the actual $V_{CE(SAT)}$, that is, the collector-emitter voltage of a transistor operating in the saturation region. Instead, it is important to know that for the bias conditions of interest, the collector-emitter voltage is less than a specified value. The circuit designer would have assumed this value, probably from knowledge of

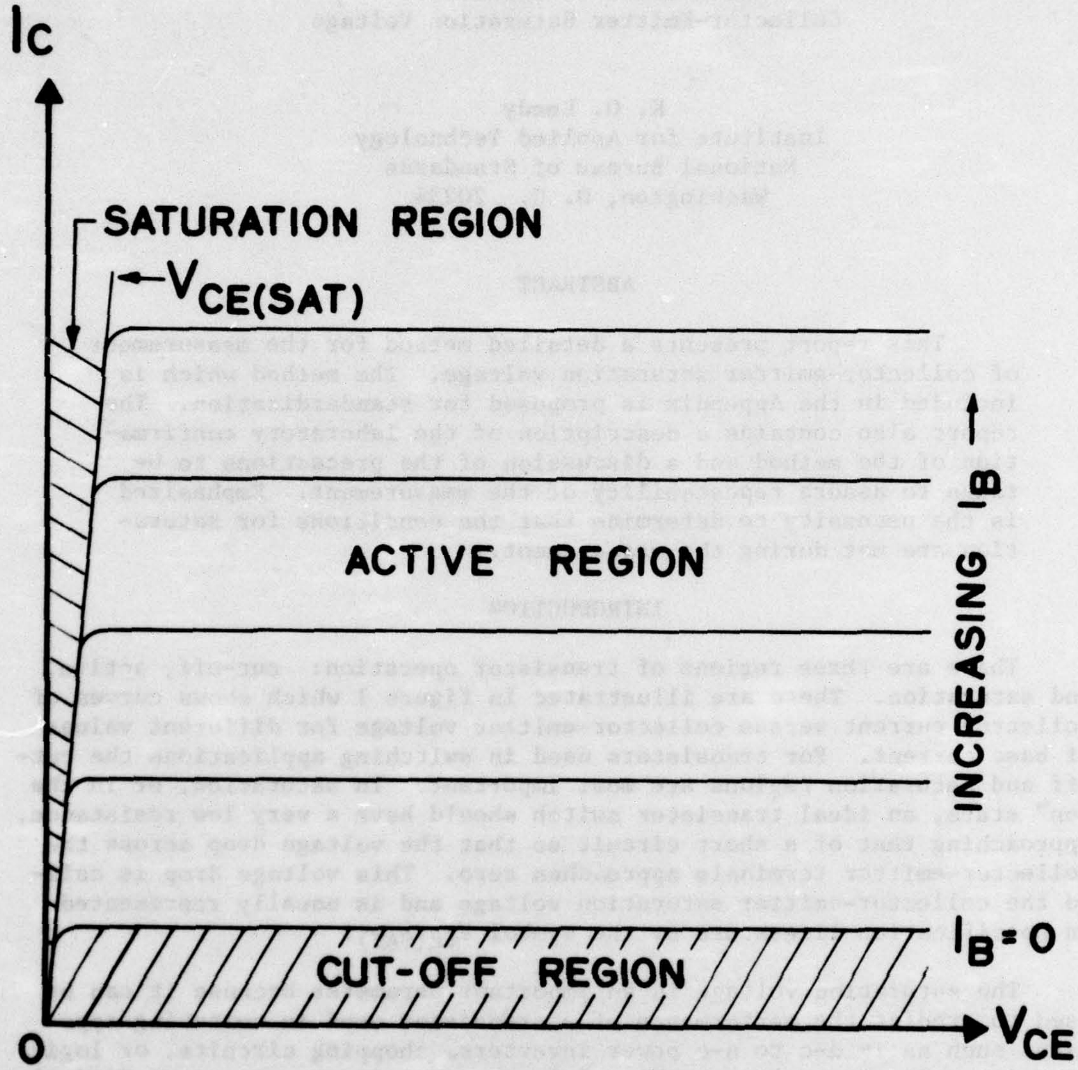

Figure 1. Illustration of the three transistor operating regions: cut-off, active, and saturation.

$V_{CE(SAT)}$ for that transistor type. The measurement method attached can be used to determine if a particular transistor will meet the requirement if the test for saturation is omitted.

From the diagram in figure 1, it is apparent that saturation is a region and that $V_{CE(SAT)}$ is not a single point but rather a line. Its value depends on the collector current and base current among other variables. The purpose of the measurement presented here is to adequately define all variables so that a repeatable measurement of $V_{CE(SAT)}$ is possible. The method itself is given in the Appendix. It can be used for any $V_{CE(SAT)}$ measurement but it is most useful when a measurement of a change in $V_{CE(SAT)}$ is required. Normally, when $V_{CE(SAT)}$ is measured, it is for the purpose of assuring that it be less than a maximum voltage in a specification. This implies that better devices have lower values of $V_{CE(SAT)}$. Therefore, it is to the advantage of the manufacturer to report a low value. To perform his measurement, he then need only control his parameters to the extent that he obtains a measured value of $V_{CE(SAT)}$ low enough to meet the specification. To measure a change in $V_{CE(SAT)}$, however, it is necessary to make the measurement twice with all important independent variables specified and carefully controlled.

DEFINITION OF SATURATION

By definition,[1] a transistor is operating in the saturation region when both the emitter-base and the collector-base junctions are forward-biased. The collector-emitter voltage in this condition has two components: the junction saturation voltage, defined below, and the voltages due to the collector saturation current in the collector series resistance and due to the emitter current in the emitter series resistance. The base series resistance can be neglected.

The junction saturation voltage is the difference between the forward-biased junction voltages of the collector-base and the emitter-base junctions. It is given by the Ebers and Moll[2] expression as:

$$\Delta V_j = \frac{kT}{q} \ln \frac{\alpha_I \left[1 - \frac{I_C}{I_B} \frac{1 - \alpha_N}{\alpha_N} \right]}{1 + \frac{I_C}{I_B} (1 - \alpha_I)}$$

where

ΔV_j = junction saturation voltage, V

T = absolute temperature, K

α_N = common base large signal d-c current gain with the emitter functioning as an emitter and the collector functioning as a collector

α_I = common base large signal d-c current gain with the emitter functioning as a collector and the collector functioning as an emitter

I_C = collector current, A

I_B = base current, A

k = Boltzman's constant (1.381×10^{-23} J/K)

q = charge on electron (1.602×10^{-19} C).

The saturation voltage is then given by

$$V_{CE(SAT)} = \Delta V_j + I_C r_C + I_E r_E$$

where

r_C = collector series resistance, Ω

r_E = emitter series resistance, Ω.

The junction saturation voltage is normally small and rather insensitive to variations in collector or base current because of the logarithmic relation. Of more significance, particularly for power transistors, is the saturation voltage due to the resistive component. The collector region of many power transistors is lightly doped to obtain high breakdown voltages and the transistor is usually operated at high currents in saturation. Under conditions which affect $V_{CE(SAT)}$, such as an increase in temperature or an exposure to radiation, the effect on the collector resistance can produce a major change in $V_{CE(SAT)}$, as can the effects of variations in transistor gain.

MEASUREMENT METHOD

The method for measuring $V_{CE(SAT)}$ as outlined in the Appendix requires that the following measurement conditions be specified:

1) I_C - the collector current

2) I_B - the base current

3) ambient temperature

4) selection of a pulsed or d-c method, and

5) the pulse width and duty cycle (if other than 300 μs and 2%, respectively).

This information must be included in the specification for $V_{CE(SAT)}$ for the particular device to be tested, such as in the detailed specifi-

cation in the appropriate military standard, if the specification is to be meaningful. The method instructs the user how to determine all circuit values. It describes all necessary apparatus, procedural steps to be performed, data to be taken, and cautions to be observed.

Using this method, several experiments were performed to determine the sensitivity of the measured $V_{CE(SAT)}$ to several variables. Three transistor types were chosen for these experiments: a small-signal transistor (2N2222), a single-diffused power transistor (2N3055), and a triple-diffused power transistor (2N5840). These devices are found in military systems and each is available in a military version. These device types were selected to provide a wide variation in measured results for variations in the measurement parameters. Three devices of each type were used for each experiment. All were off-the-shelf commercial transistors. Though the number of devices used is small, the data indicate the trends in the effects of the variables and, as such, indicate which parameters are necessary to control carefully and which are not.

TEMPERATURE EFFECTS

The value of $V_{CE(SAT)}$ is dependent on temperature in at least two ways: first, temperature appears in the expression for the junction saturation voltage, and second, the collector series resistance is a function of temperature. The method specifies that the measurement be made at a nominal temperature of 20°C and that the power levels used do not give rise to significant heating of the junction. To investigate the effects of elevated temperature on the value of $V_{CE(SAT)}$, the following experiments were performed.

To simulate a rise in the ambient temperature, the transistors were placed in a heated oil bath whose temperature was controlled at approximately 10°C intervals from room temperature to 100°C during measurement of $V_{CE(SAT)}$. Sufficient time was allowed for the transistor to reach a steady-state temperature between measurements.

Figure 2 shows the measured value of $V_{CE(SAT)}$ versus temperature for the three transistor types studied. In each case the base current was pulsed with a 2% duty cycle and a pulse width of 300 μs. Both the 2N2222, figure 2a, and 2N3055, figure 2b, show a small increase in $V_{CE(SAT)}$ with temperature while the 2N5840, figure 2c, shows a much greater increase. It is to be expected that the 2N5840 would be much more sensitive to temperature since it is designed to have a very high breakdown voltage. In order to have a high breakdown voltage, the collector region has a very low doping level which provides a high collector series resistance with a high temperature coefficient. To compare the performance of the three transistor types, the data in figure 2 was plotted in figure 3 as percentage change in $V_{CE(SAT)}$ from its value at room temperature as a function of temperature. In this case the percent change in $V_{CE(SAT)}$ is

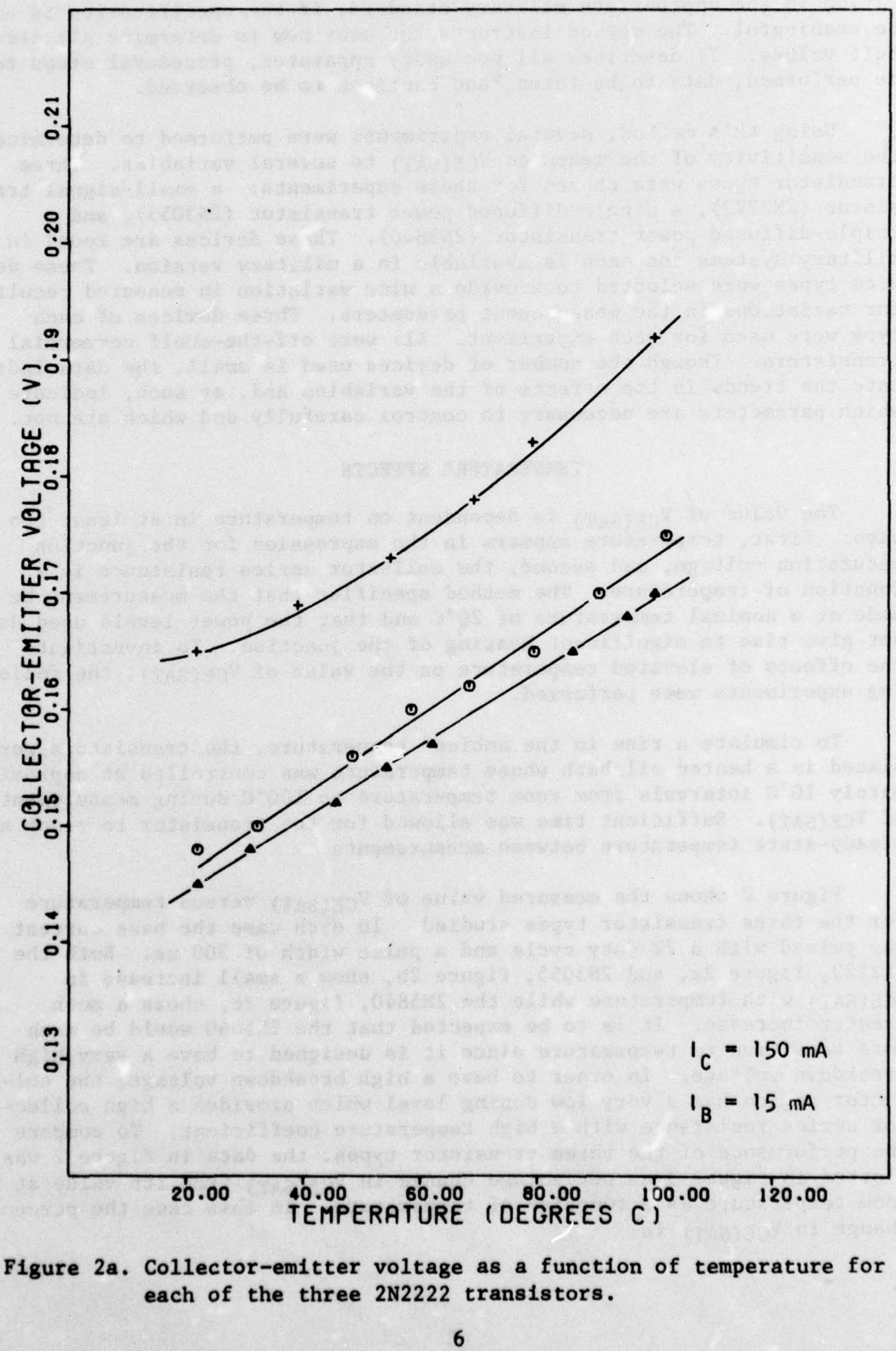

Figure 2a. Collector-emitter voltage as a function of temperature for each of the three 2N2222 transistors.

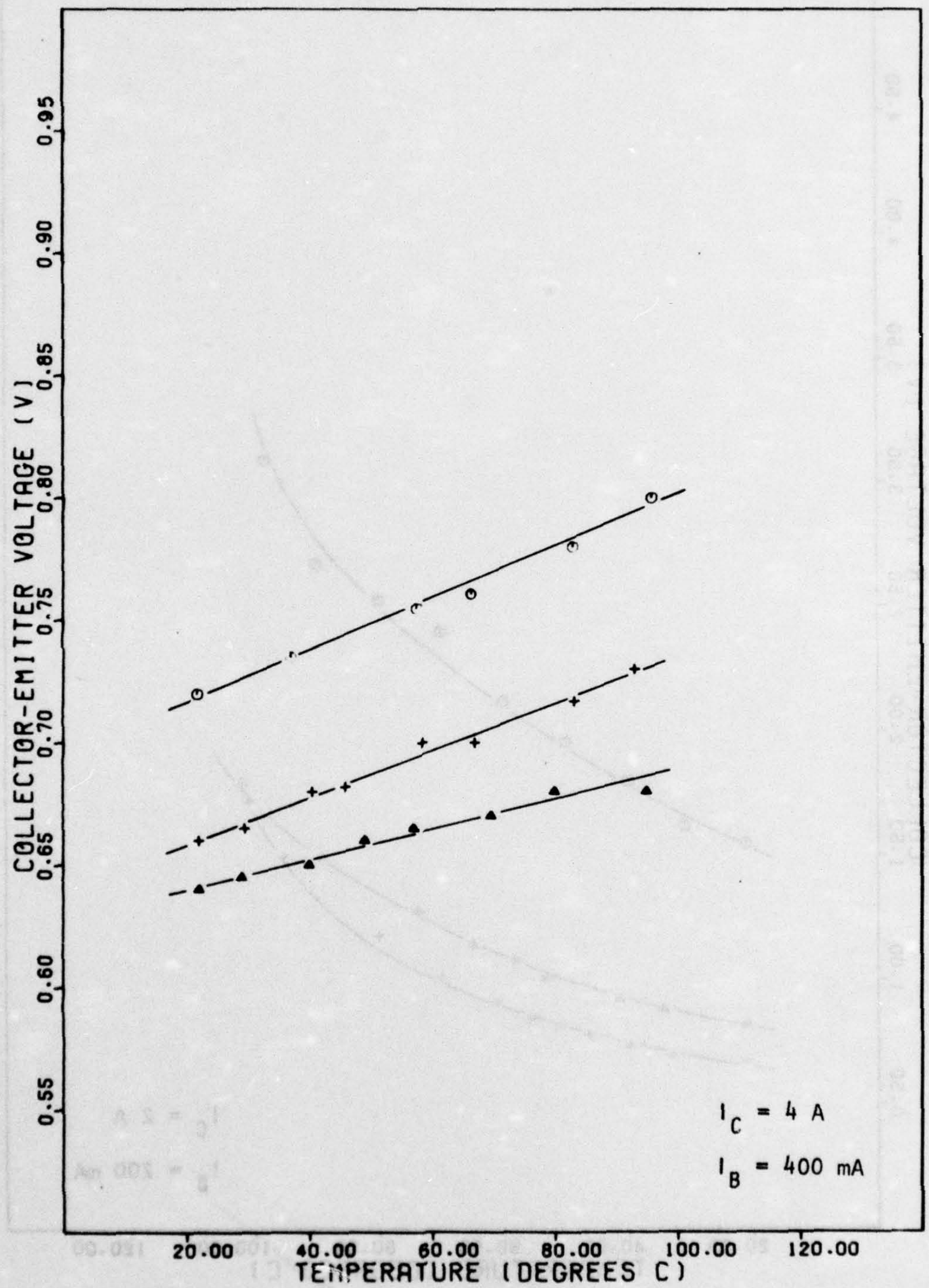

Figure 2b. Collector-emitter voltage as a function of temperature for each of the three 2N3055 transistors.

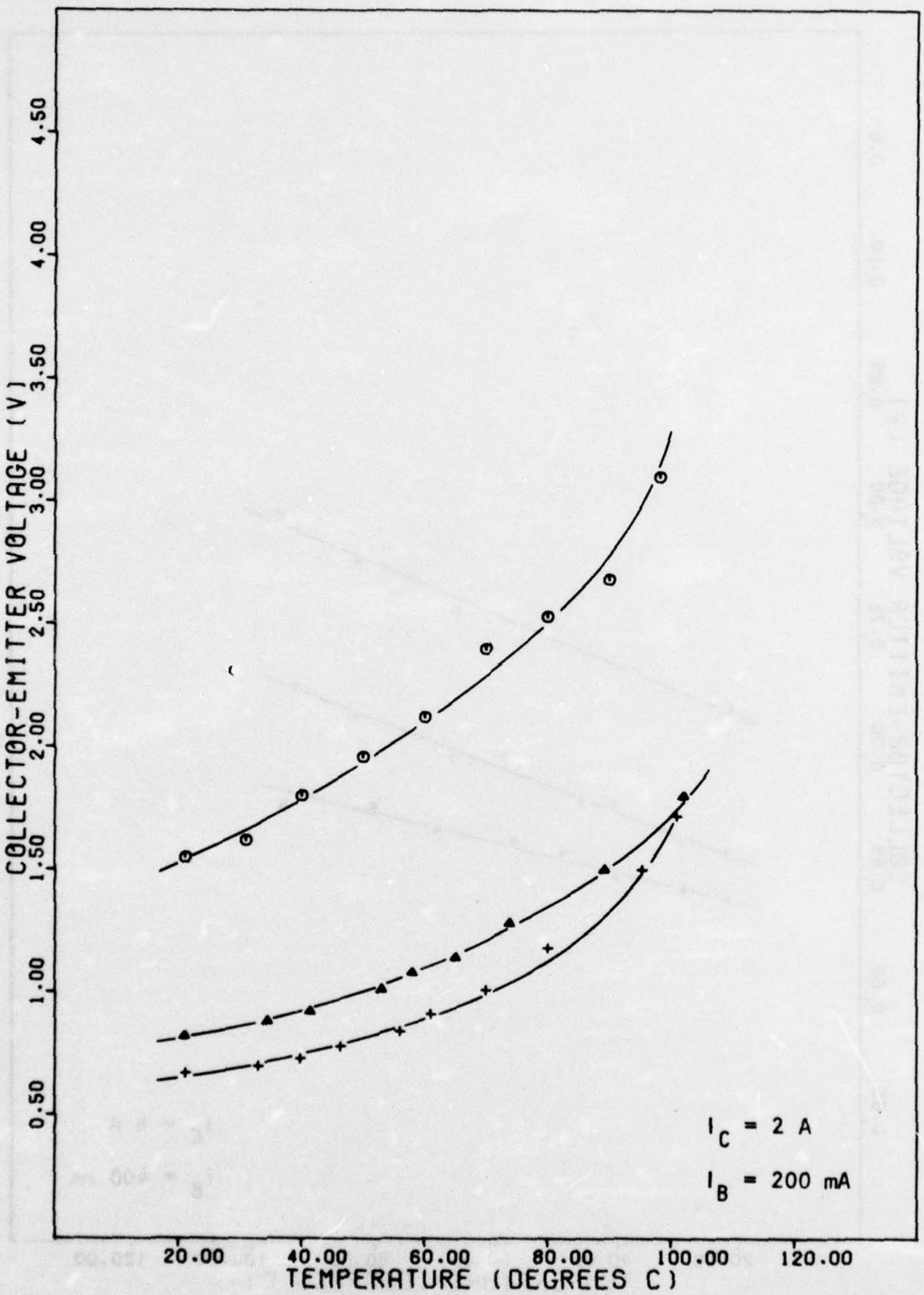

Figure 2c. Collector-emitter voltage as a function of temperature for each of the three 2N5840 transistors.

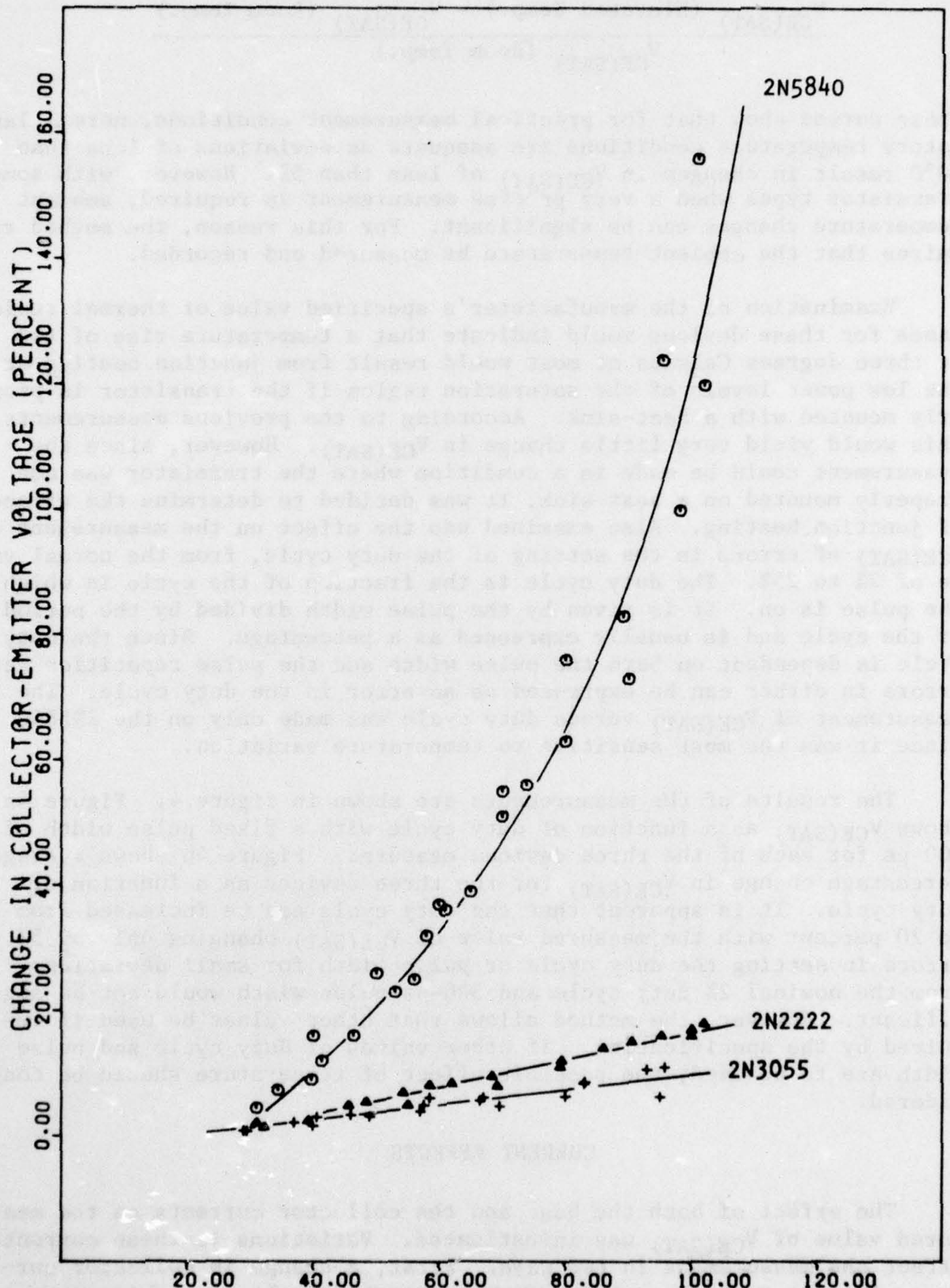

Figure 3. Typical change in collector-emitter voltage as a function of temperature for the three device types with the data averaged for the three samples of each type.

$$\frac{V_{CE(SAT)}\ (\text{Elevated Temp.}) - V_{CE(SAT)}\ (\text{Room Temp.})}{V_{CE(SAT)}\ (\text{Room Temp.})}$$

These curves show that for practical measurement conditions, normal laboratory temperature conditions are adequate as deviations of less than 10°C result in changes in $V_{CE(SAT)}$ of less than 5%. However, with some transistor types when a very precise measurement is required, ambient temperature changes can be significant. For this reason, the method requires that the ambient temperature be measured and recorded.

Examination of the manufacturer's specified value of thermal resistance for these devices would indicate that a temperature rise of two or three degrees Celsius at most would result from junction heating at the low power levels of the saturation region if the transistor is properly mounted with a heat-sink. According to the previous measurements, this would yield very little change in $V_{CE(SAT)}$. However, since the measurement could be made in a condition where the transistor was not properly mounted on a heat-sink, it was decided to determine the effect of junction heating. Also examined was the effect on the measurement of $V_{CE(SAT)}$ of errors in the setting of the duty cycle, from the normal value of 2% to 25%. The duty cycle is the fraction of the cycle in which the pulse is on. It is given by the pulse width divided by the period of the cycle and is usually expressed as a percentage. Since the duty cycle is dependent on both the pulse width and the pulse repetition rate, errors in either can be expressed as an error in the duty cycle. The measurement of $V_{CE(SAT)}$ versus duty cycle was made only on the 2N5840 since it was the most sensitive to temperature variation.

The results of the measurements are shown in figure 4. Figure 4a shows $V_{CE(SAT)}$ as a function of duty cycle with a fixed pulse width of 300 μs for each of the three devices measured. Figure 4b shows average percentage change in $V_{CE(SAT)}$ for the three devices as a function of duty cycle. It is apparent that the duty cycle can be increased from 2 to 20 percent with the measured value of $V_{CE(SAT)}$ changing only by 5%. Errors in setting the duty cycle or pulse width for small deviations from the nominal 2% duty cycle and 300-μs pulse width would not be significant. However, the method allows that other values be used if required by the specification. If other values of duty cycle and pulse width are to be used, the possible effect of temperature should be considered.

CURRENT EFFECTS

The effect of both the base and the collector currents on the measured value of $V_{CE(SAT)}$ was investigated. Variations in these currents affect the measurement in two ways. First, a change in collector current will alter the $I_C r_C$ term of the saturation voltage. This can produce a change in the measured value of $V_{CE(SAT)}$ approximately proportional to the change in collector current. Second, changing either current can cause the transistor to operate in the active region instead of the saturation region. This will increase the measured value of V_{CE} by sev-

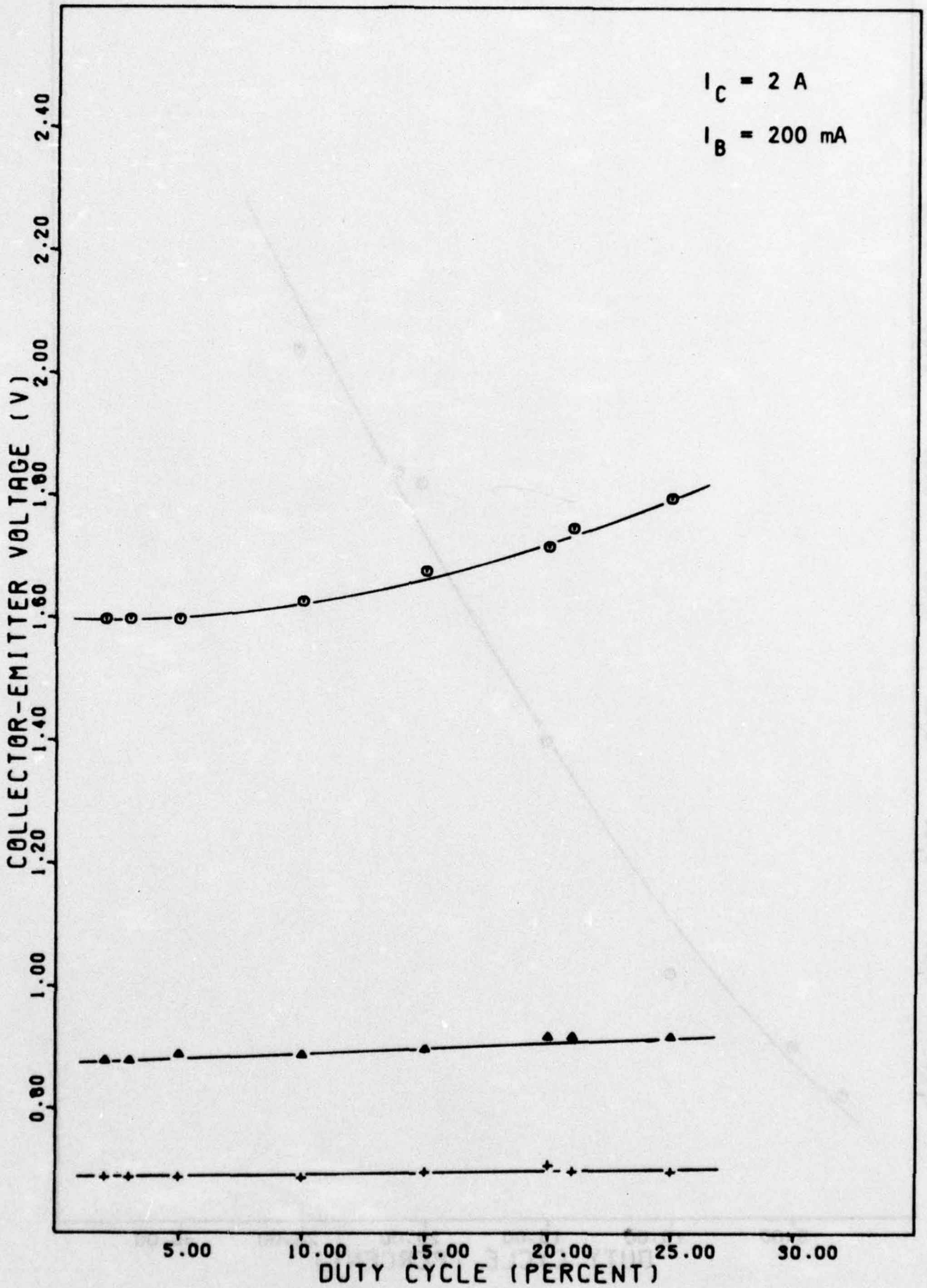

Figure 4a. Collector-emitter voltage as a function of duty cycle for each of the three 2N5840 transistors.

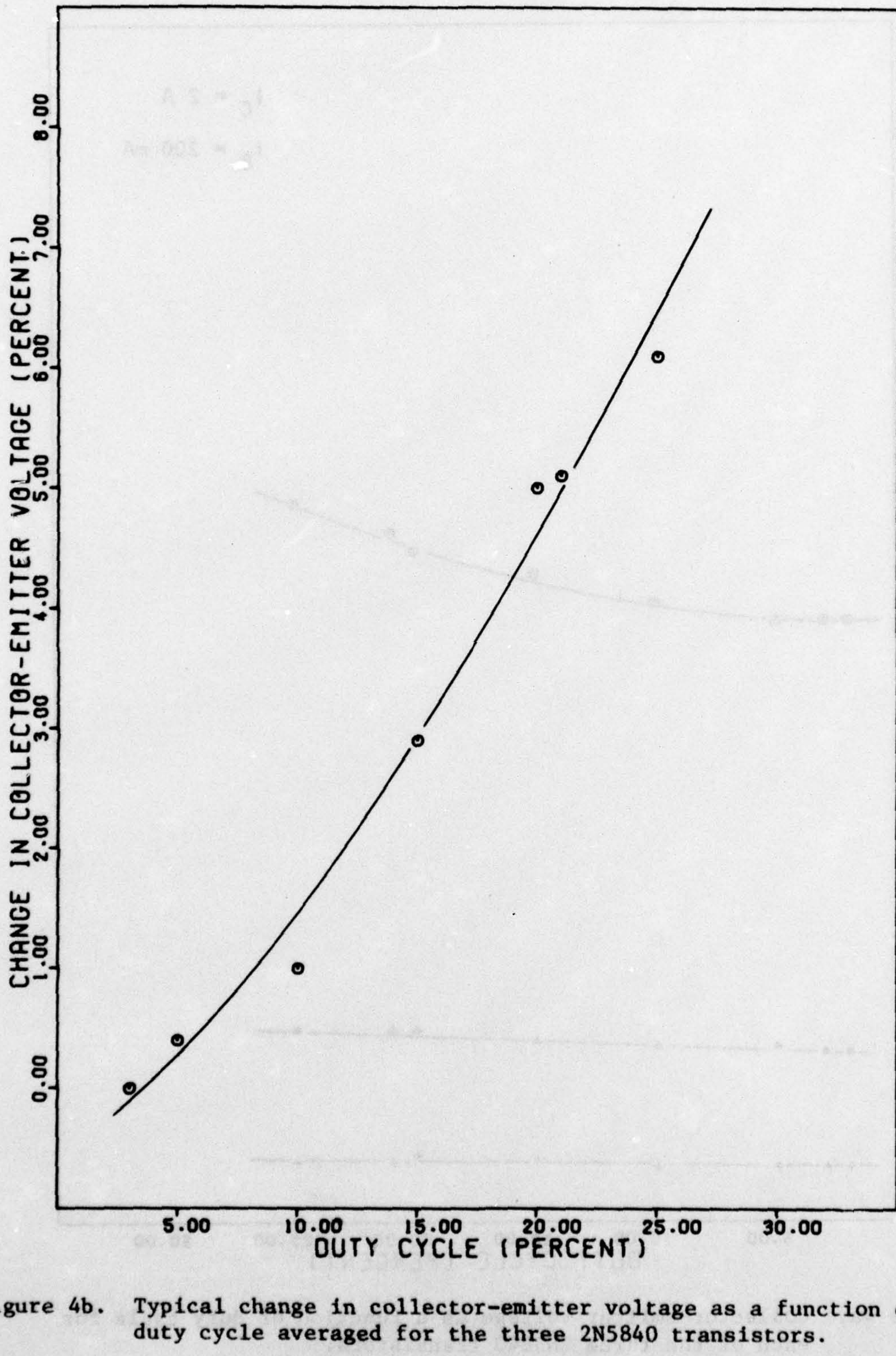

Figure 4b. Typical change in collector-emitter voltage as a function of duty cycle averaged for the three 2N5840 transistors.

eral hundred percent for changes in I_C of only tens of percent. Obviously, this value of collector-emitter voltage is not $V_{CE(SAT)}$. Assuring that the transistor is indeed operating in the saturation region during the measurement of $V_{CE(SAT)}$ is of utmost importance.

As was indicated earlier, the definition of saturation is when both the collector-base and the emitter-base junctions are forward-biased. In practice the bias conditions to assure saturation are difficult to determine. It is more convenient to observe the gain to determine saturation. The d-c common emitter current gain, β, is the ratio of I_C to I_B. When the transistor is operating in the saturation region, this ratio is referred to as the forced gain, since both I_C and I_B are set in order to force the transistor to operate in saturation. It is convenient to consider a transistor to be in saturation if

$$\beta_{forced} << \beta_{active}.$$

Measurements were made of V_{CE} as a function of base and collector currents for the three transistor types. The base and collector currents were sensed with a current transformer, the output of which was viewed on an oscilloscope. As outlined in the method, the current could have been measured by using an oscilloscope with a differential input to measure voltage across resistors in series with the base and the collector.

The results of varying I_C with I_B fixed are shown for the 2N2222 in figure 5a, for the 2N3055 in figure 5b, and the 2N5840 in figure 5c. In each case the value chosen for I_B was the value required in the detailed military specification. The value required for I_C in that specification is indicated by an arrow in each case. The data are combined in figure 6 which shows the percentage change in V_{CE} versus percentage change in I_C for the three transistor types. Each data point represents the average value for the three devices sampled. Similar curves of V_{CE} versus I_B, with I_C constant, are shown in figure 7. Figure 8 shows the results combined. Again, in each case, the value which was fixed for I_C is from the detailed military specification and the I_B value required in that specification is noted.

The results show that V_{CE} is sensitive to both I_C and I_B in most cases. Errors in measuring these currents can result in significant errors in the measured value of $V_{CE(SAT)}$. For this reason the method stresses the necessity of making accurate measurements of these currents. The portion of the curves where the slope is very steep represents operation of the transistor in or very near the active region. A measurement of V_{CE} here is not of $V_{CE(SAT)}$. When I_B and I_C (or the forced β) are selected in the specification for this method, care should be taken so that this measurement is made well within the saturation region so that errors in setting the currents will not cause the measurement to be made in the active region. For the three transistor types used in this report, the value of forced β given in the detailed specification of the military standard is 10 in each case. That is, the $V_{CE(SAT)}$ measurement is made with an I_C to I_B ratio of 10. This is the same value chosen for

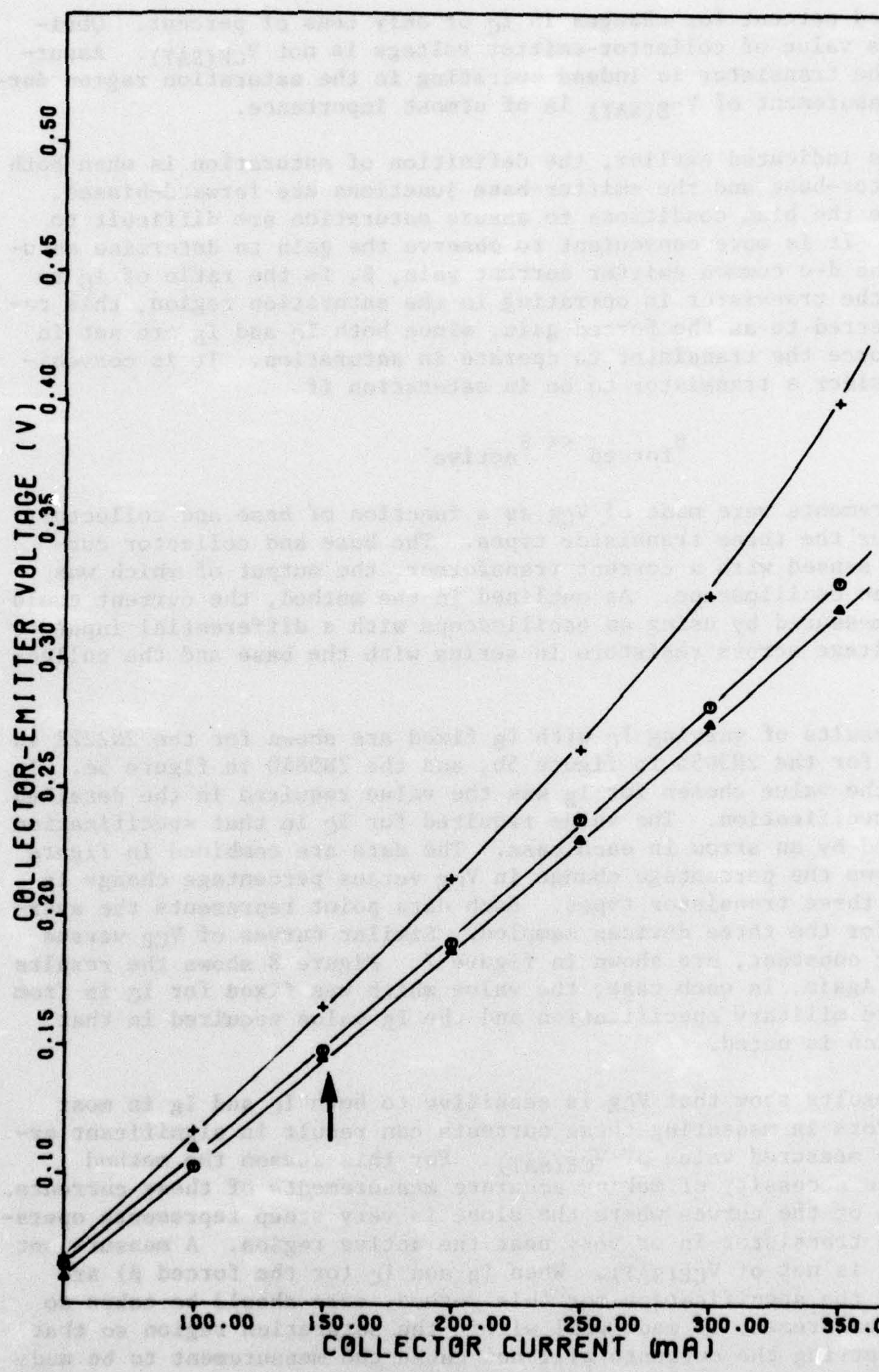

Figure 5a. **Collector-emitter voltage as a function of collector current with a fixed base current of 15 mA for each of the three 2N2222 transistors.**

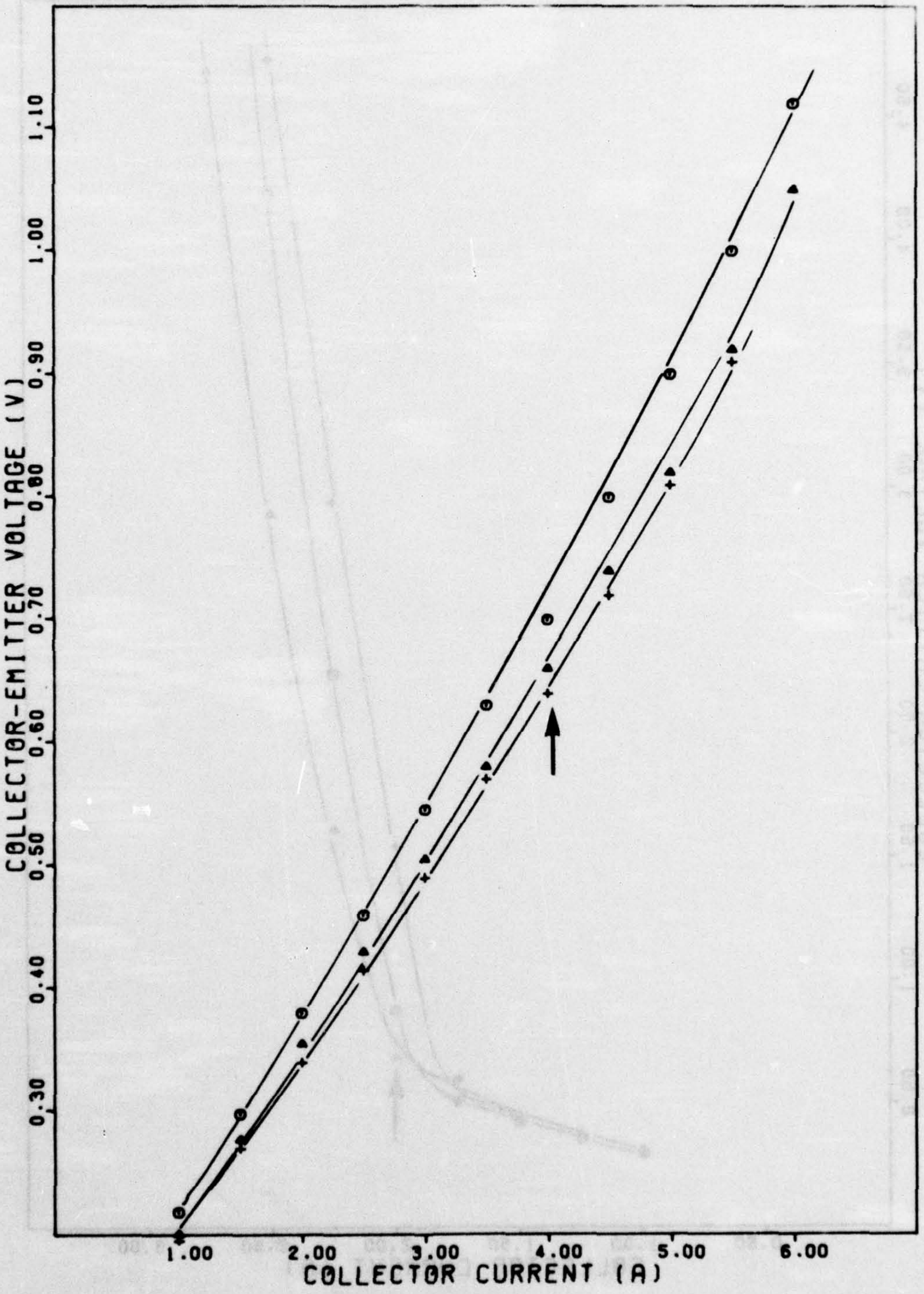

Figure 5b. Collector-emitter voltage as a function of collector current with a fixed base current of 400 mA for each of the three 2N3055 transistors.

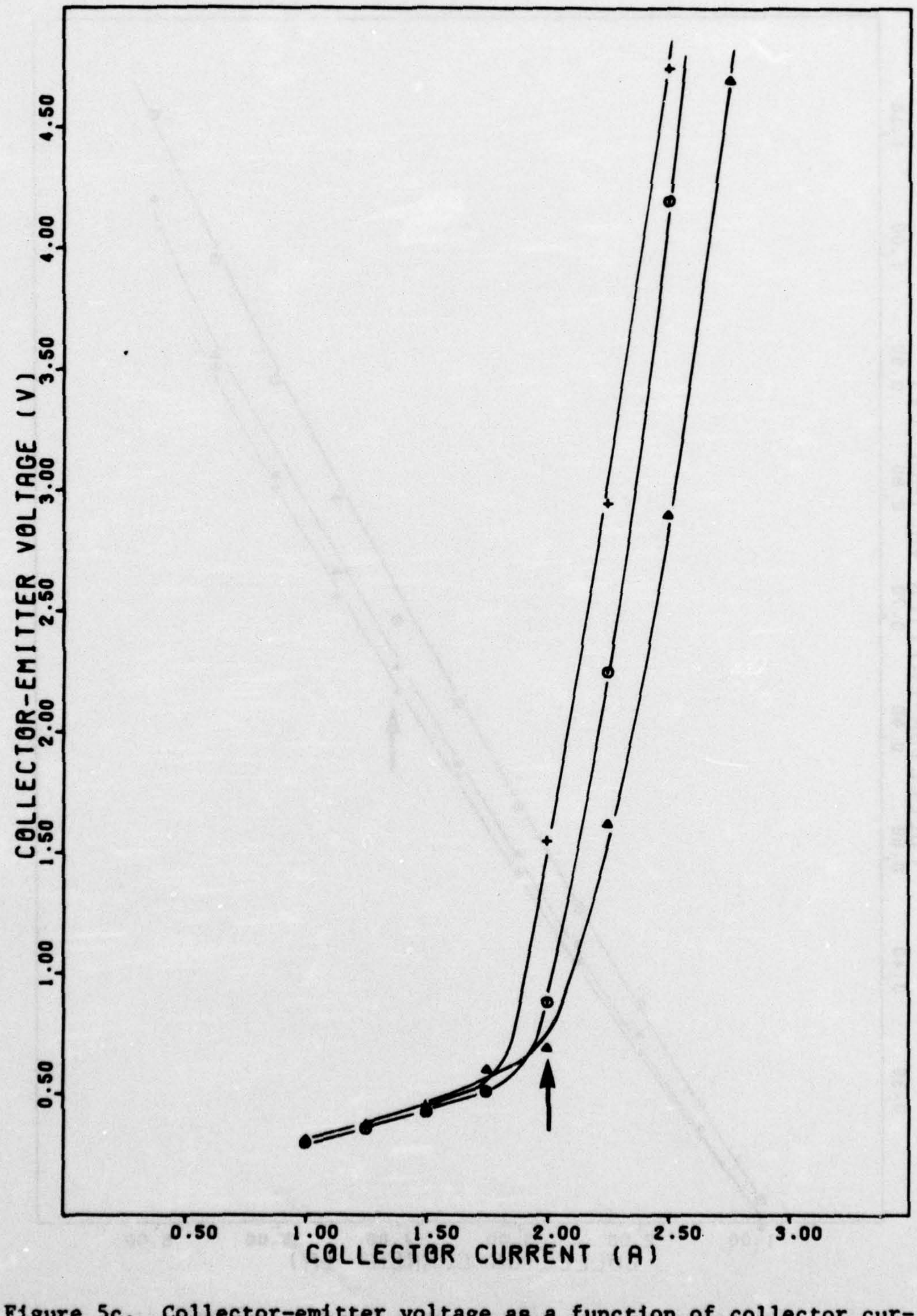

Figure 5c. Collector-emitter voltage as a function of collector current with a fixed base current of 200 mA for each of the three 2N5840 transistors.

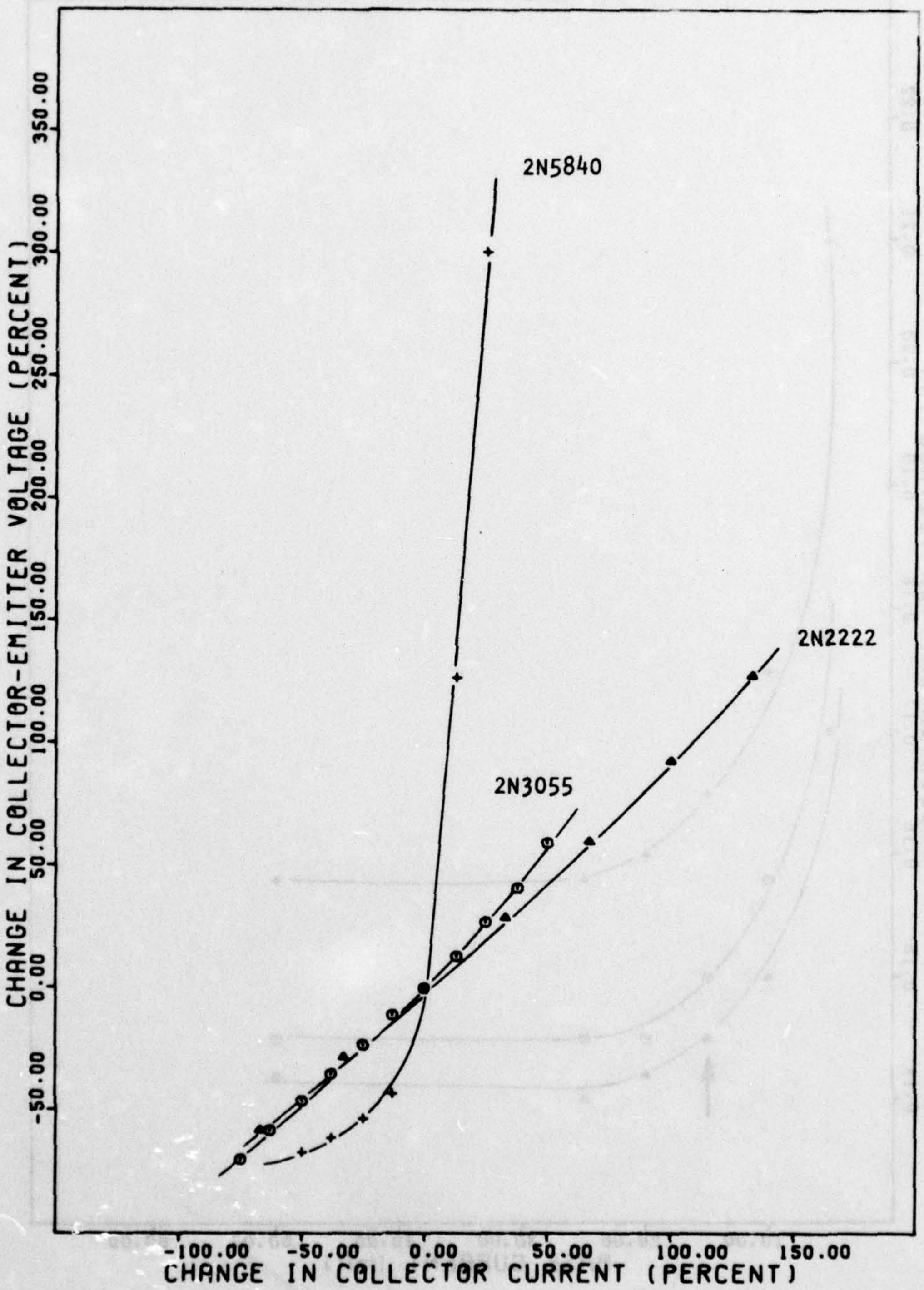

Figure 6. Typical change in collector-emitter voltage as a function of change in collector current.

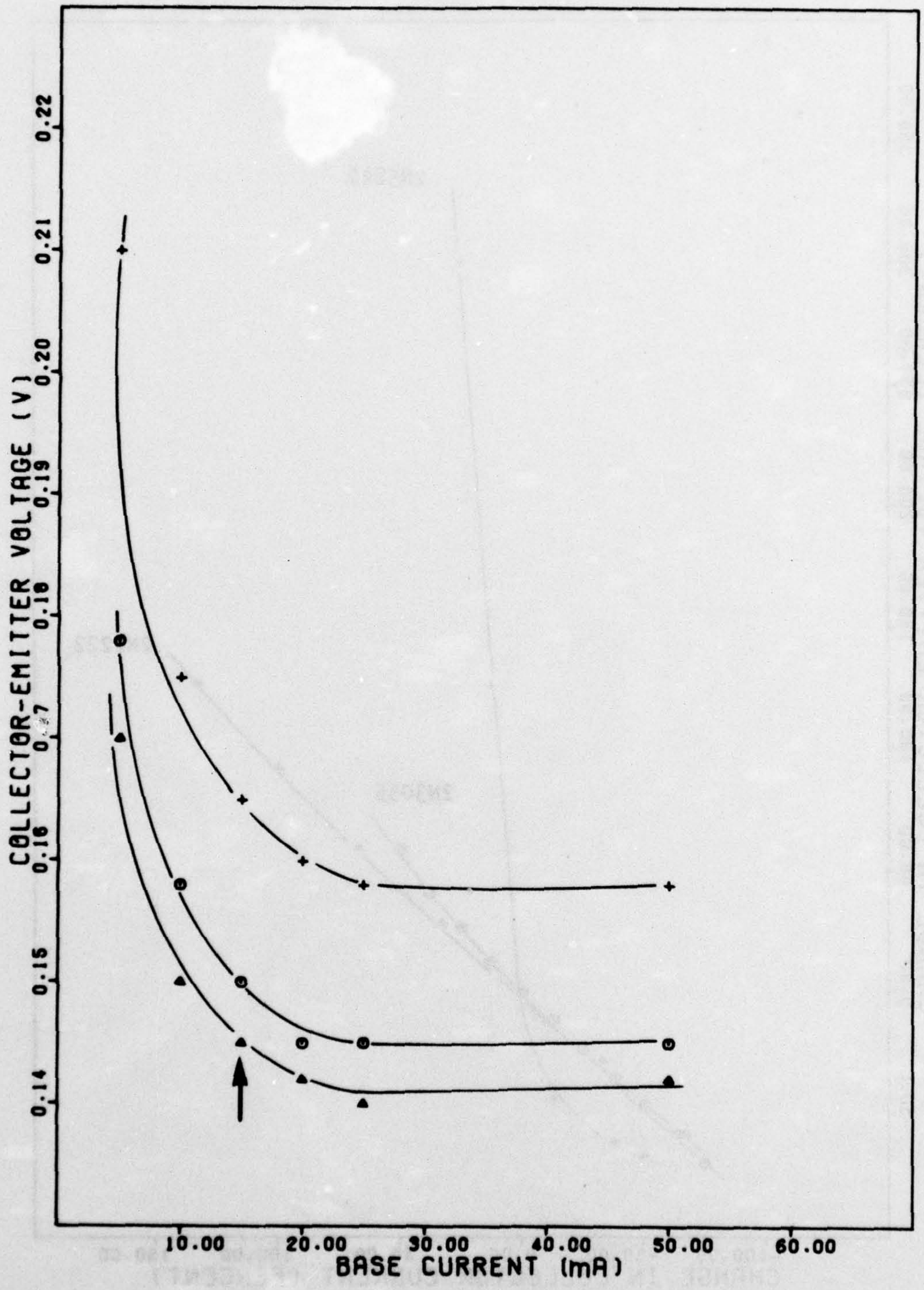

Figure 7a. Collector-emitter voltage as a function of base current with a fixed collector current of 150 mA for each of the three 2N2222 transistors.

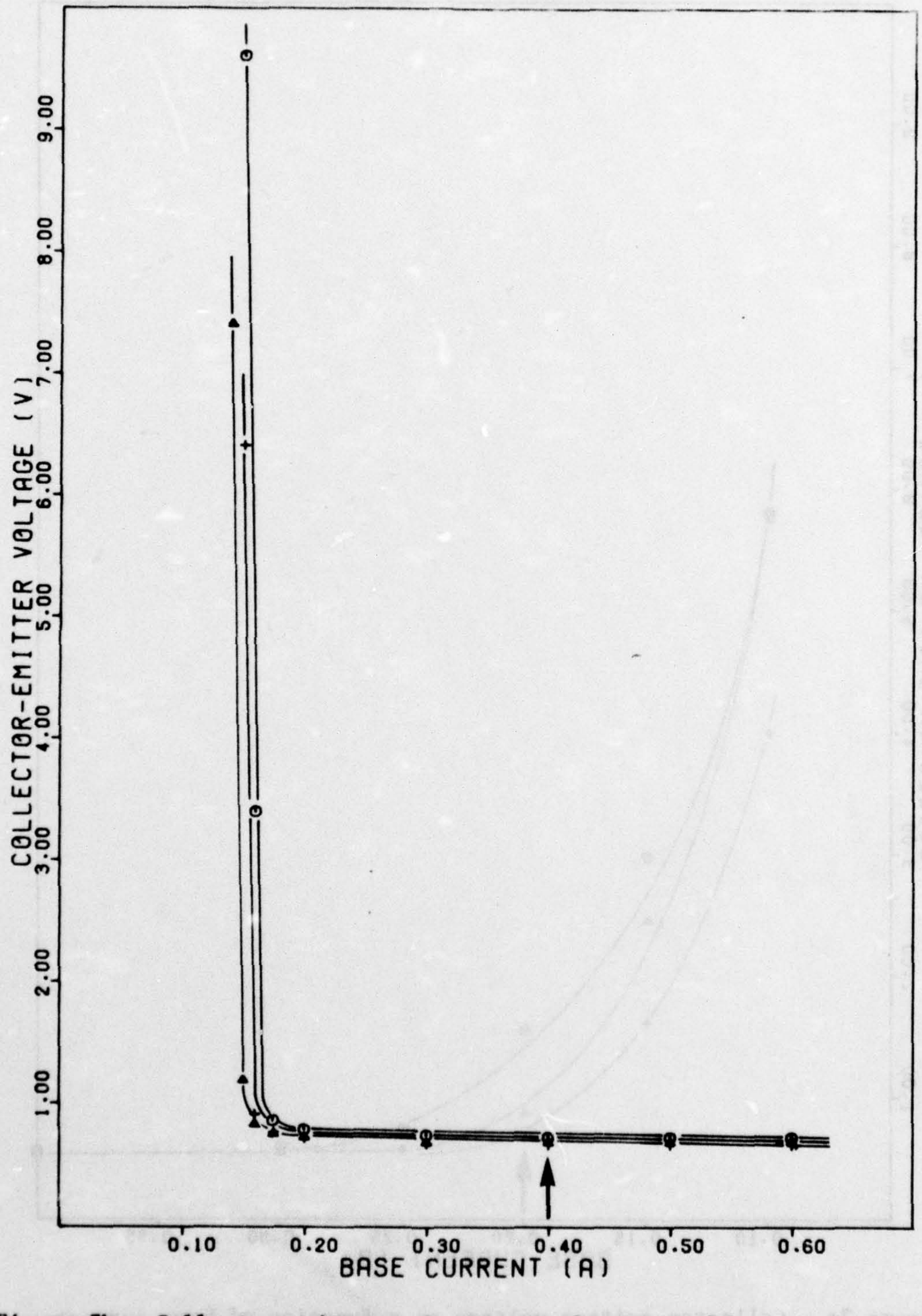

Figure 7b. Collector-emitter voltage as a function of base current with a fixed collector current of 4 A for each of the three 2N3055 transistors.

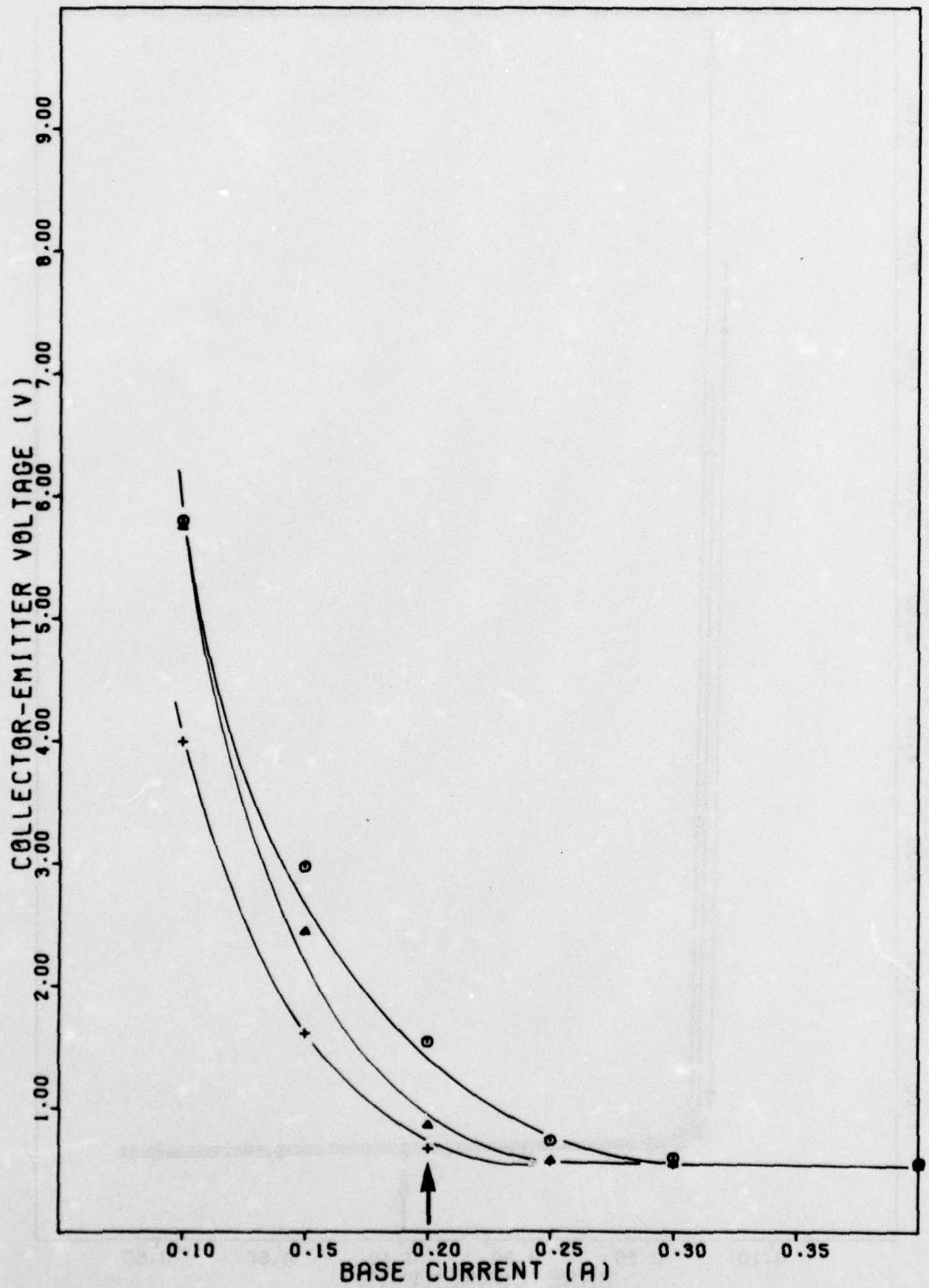

Figure 7c. Collector-emitter voltage as a function of base current with a fixed collector current of 2 A for each of the three 2N5840 transistors.

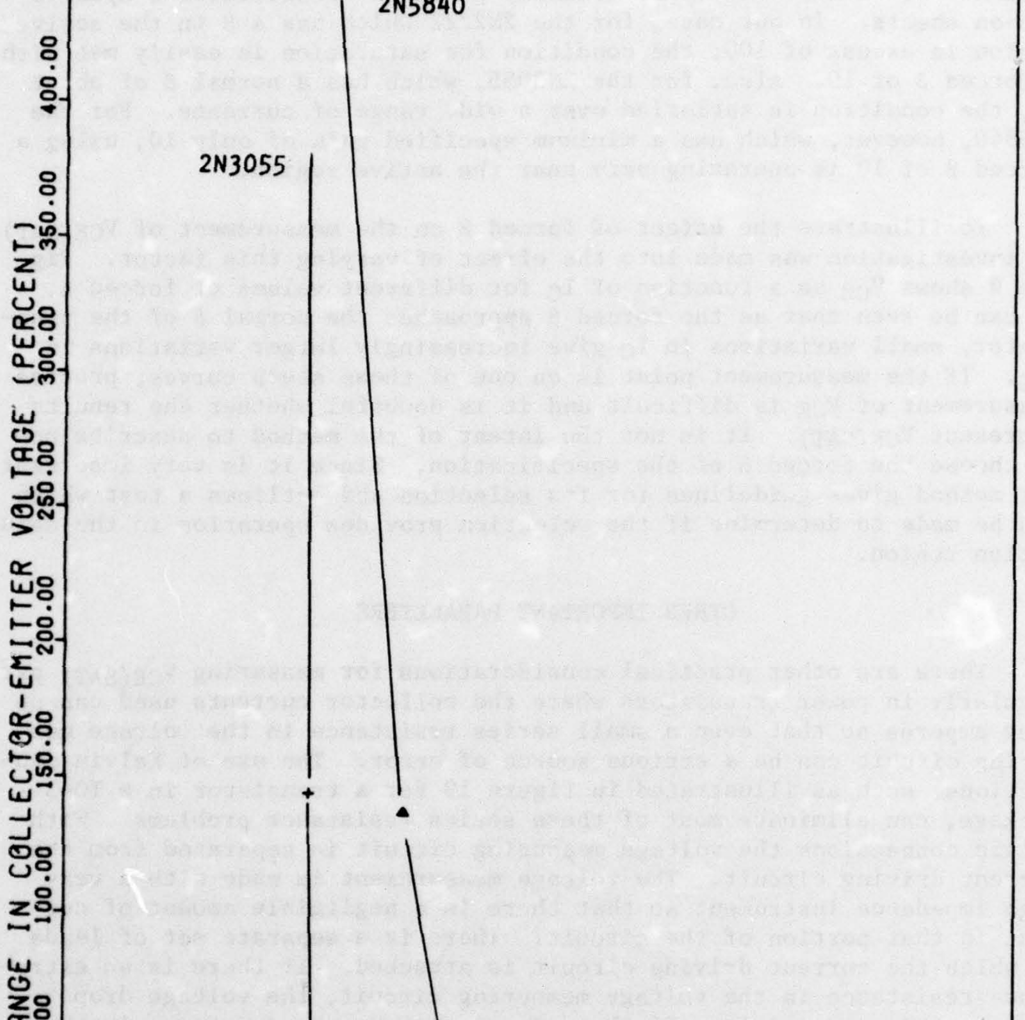

Figure 8. Typical change in collector-emitter voltage as a function of change in base current.

nearly every transistor for which there is a detailed military specification. It is also the ratio commonly given on manufacturer's specification sheets. In our case, for the 2N2222 which has a β in the active region in excess of 100, the condition for saturation is easily met with a forced β of 10. Also, for the 2N3055, which has a normal β of about 50, the condition is satisfied over a wide range of currents. For the 2N5840, however, which has a minimum specified gain of only 10, using a forced β of 10 is operating very near the active region.

To illustrate the effect of forced β on the measurement of $V_{CE(SAT)}$, an investigation was made into the effect of varying this factor. Figure 9 shows V_{CE} as a function of I_C for different values of forced β. It can be seen that as the forced β approaches the normal β of the transistor, small variations in I_C give increasingly larger variations in V_{CE}. If the measurement point is on one of these steep curves, precise measurement of V_{CE} is difficult and it is doubtful whether the results represent $V_{CE(SAT)}$. It is not the intent of the method to describe how to choose the forced β of the specification. Since it is very important, the method gives guidelines for its selection and outlines a test which can be made to determine if the selection provides operation in the saturation region.

OTHER IMPORTANT PARAMETERS

There are other practical considerations for measuring $V_{CE(SAT)}$ particularly in power transistors where the collector currents used can be many amperes so that even a small series resistance in the voltage measuring circuit can be a serious source of error. The use of Kelvin connections, such as illustrated in figure 10 for a transistor in a TO-3 package, can eliminate most of these series resistance problems. With Kelvin connections the voltage measuring circuit is separated from the current driving circuit. The voltage measurement is made with a very high impedance instrument so that there is a negligible amount of current in that portion of the circuit. There is a separate set of leads to which the current driving circuit is attached. If there is an extraneous resistance in the voltage measuring circuit, the voltage drop across it is negligible. If there is an extraneous resistance in the current driving circuit, the voltage drop across it is not involved in the voltage measurement and therefore will not lead to an error in measuring $V_{CE(SAT)}$.

Note in figure 10 that Kelvin connections are made only to the emitter and collector leads. No voltage measurement is made in the base circuit so that Kelvin connections are not required.

The method requires Kelvin connections to be made on the collector and emitter leads for all types of transistors tested. There are perhaps transistor types which have a high $V_{CE(SAT)}$ at a low collector current for which Kelvin connections are not essential. It is difficult to incorporate into the method a means of judging when to use Kelvin connections since the possible size of an extraneous resistance is not known. Since the majority of transistor types require Kelvin connections in any

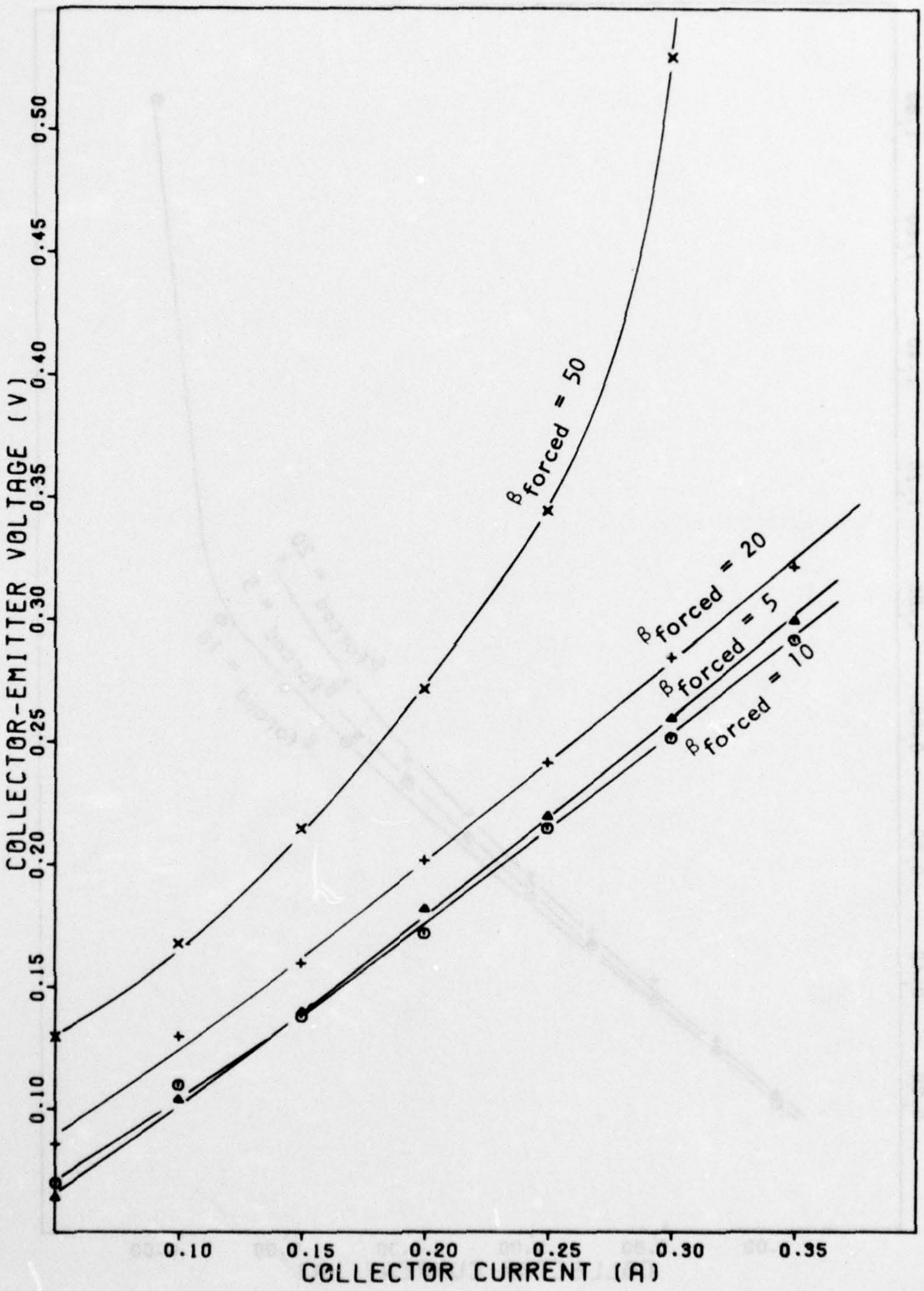

Figure 9a. Collector-emitter voltage as a function of collector current for different values of forced β for a 2N2222 transistor.

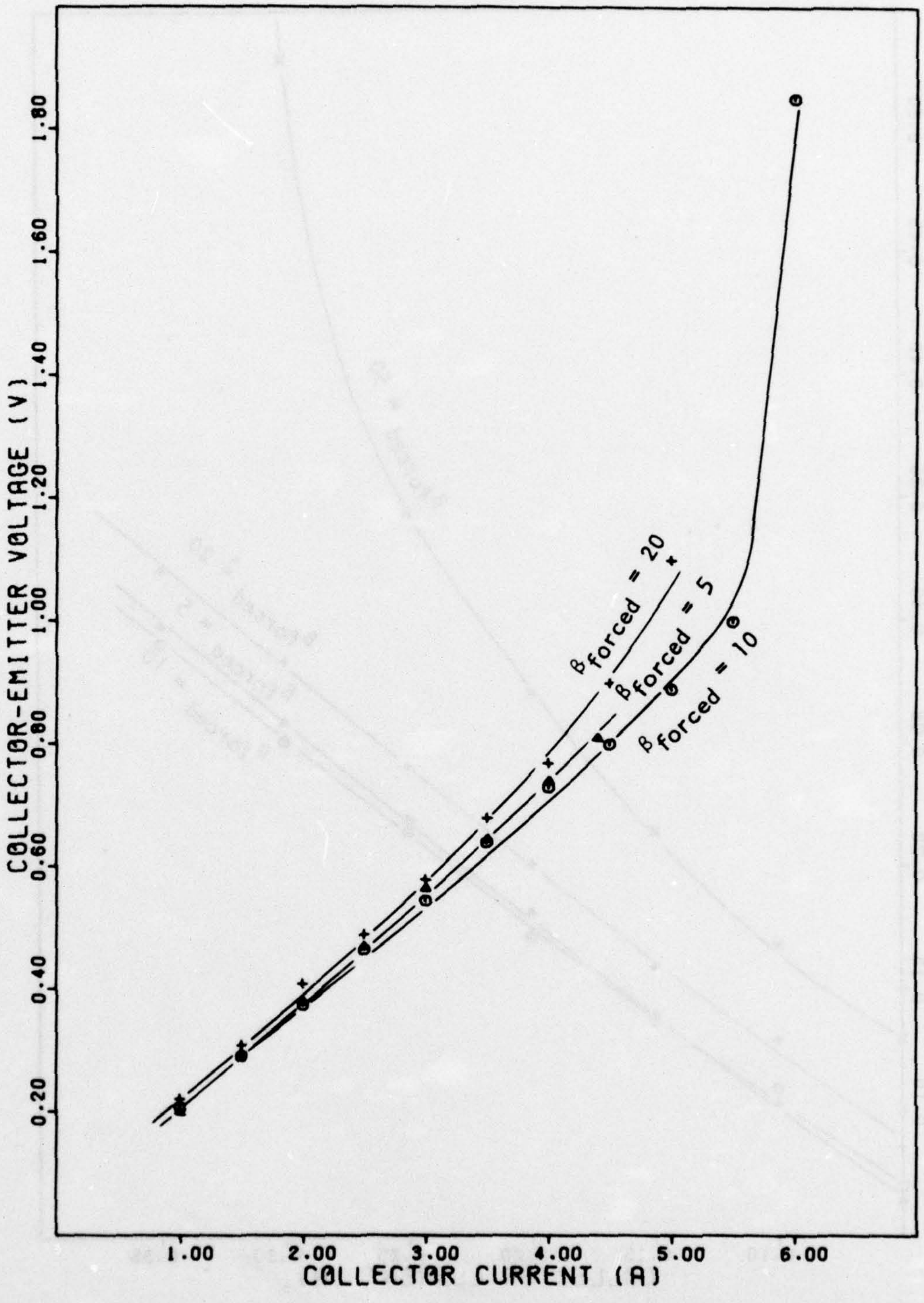

Figure 9b. Collector-emitter voltage as a function of collector current for different values of forced β for a 2N3055 transistor.

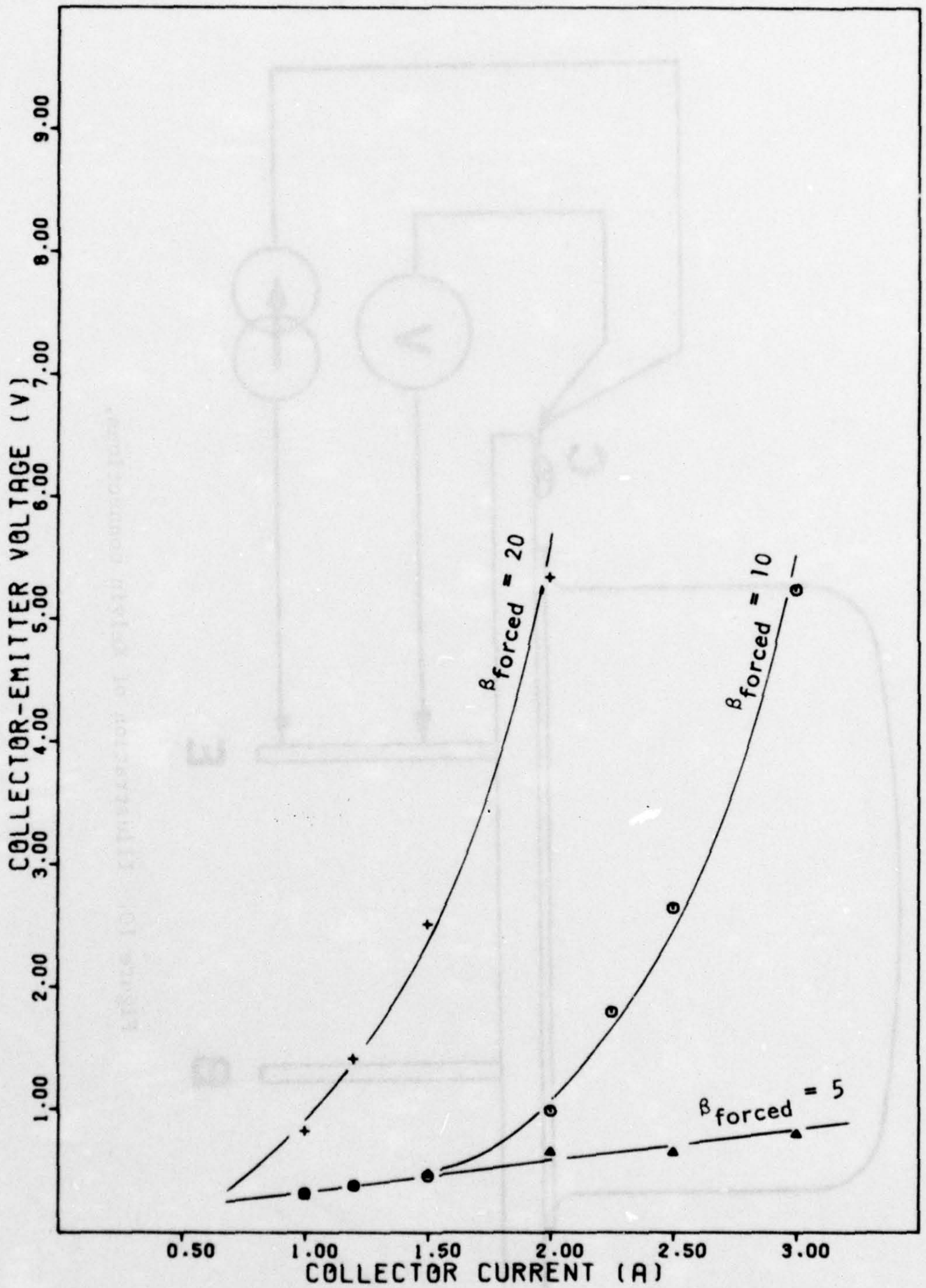

Figure 9c. Collector-emitter voltage as a function of collector current for different values of forced β for a 2N5840 transistor.

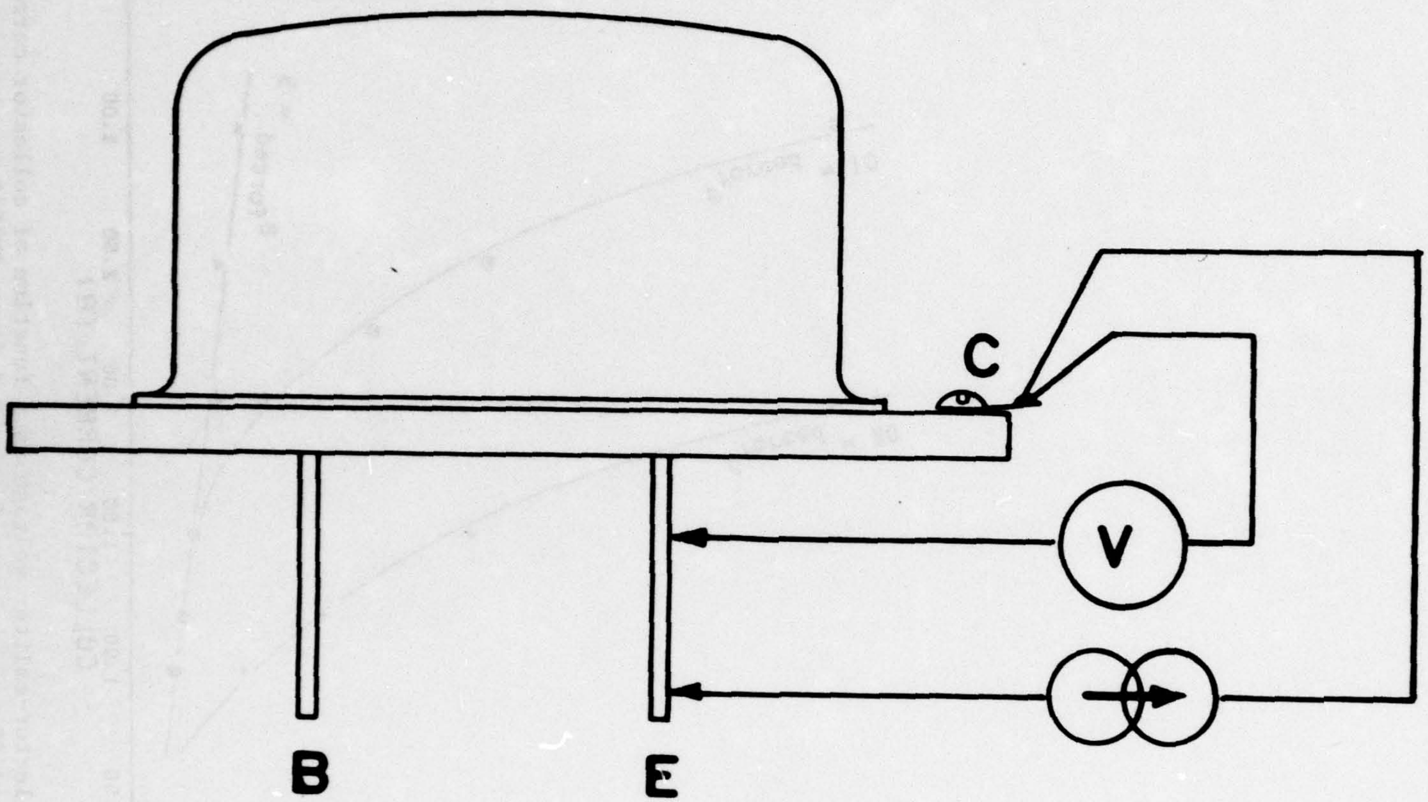

Figure 10. Illustration of Kelvin connections.

case, it is more appropriate to require their use on all transistor types.

The effect of another type of extraneous resistance is not correctable by the use of Kelvin connections. These are series resistances that occur in the circuit between the transistor and the point where the voltage sensing connection is made. The current provided by the current driving circuit will cause a voltage drop across such a resistance which will be measured by the voltage measuring circuit as part of $V_{CE(SAT)}$. An example of such a resistance is the resistance of the leads of the transistor. For this reason, the method requires that contact be made reproducibly to the transistor within 3 mm of the transistor case. Another source of resistance is contact resistance due to poor or dirty contacts. The method requires that the transistor holder have good quality contacts and that they be kept clean.

Another source of error in the measurement of $V_{CE(SAT)}$ is variations in the measurement circuit itself. The current levels used, particularly for power transistors, require considerable power dissipation in the resistors in the collector circuit. Care should be taken to select resistors that are capable of handling this power without changing resistance. In the pulsed method, a temperature drift in the resistors R_B and R_C could cause serious error in the measurement of $V_{CE(SAT)}$ because the measurement would be made at the wrong values of I_B and I_C.

When the pulsed method is used, the voltage measurement of $V_{CE(SAT)}$ must be made with an instrument capable of measuring the voltage of one portion of a pulse with respect to the ground potential. See figure 3 in the method. This measurement can be made with an oscilloscope if it is capable of accurately following the pulse from the high level which occurs when the current pulse is off to the low level of $V_{CE(SAT)}$ when the current pulse is on. If, however, the amplifiers in the oscilloscope saturate, an erroneous measurement of $V_{CE(SAT)}$ will be made. One way to avoid this is by application of a clamping circuit at the input of the oscilloscope. The effect of this circuit is to lower the voltage during the time the current pulse is off so that it is similar in magnitude to the value of $V_{CE(SAT)}$ when the current pulse is on. An oscilloscope can easily follow the new pulse shape without saturating. An example of such a circuit is shown in Appendix X2 of the method.

A clamping circuit similar to that shown was used in the $V_{CE(SAT)}$ measurements described. In order to determine if the addition of the clamping circuit caused error in the measured value of $V_{CE(SAT)}$, the current was measured in the 1000-Ω resistor. It was found to be less than 1 μA during the time the base current pulse was on and the $V_{CE(SAT)}$ measurement was being made. Therefore, the clamping circuit did not cause a measurable extraneous voltage drop to occur as part of $V_{CE(SAT)}$.

SUMMARY

A method for the measurement of $V_{CE(SAT)}$ has been outlined and discussed. It was found that the most important factor in the measurement

of $V_{CE(SAT)}$ was the selection of the forced β. Precise measurement of base and collector currents is necessary. Small temperature changes are usually not important. The use of Kelvin connections to eliminate errors due to extraneous resistances is very important. Short lead lengths on the test transistors and good quality connections and contacts should be maintained. Good quality circuit components with adequate power rating should be used.

ACKNOWLEDGMENT

D. L. Blackburn, G. J. Rogers, and T. F. Leedy have provided useful comments and suggestions in the preparation of this report.

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APPENDIX

METHODS TO MEASURE TRANSISTOR

COLLECTOR-EMITTER SATURATION VOLTAGE

Document No.:

Draft No.: 1

Date: June 1, 1977

Prepared by: K. O. Leedy
(301) 921-3625

1. Scope

1.1 These methods cover tests to determine transistor collector-emitter saturation voltage $V_{CE(SAT)}$ under specified conditions.

1.2 The d-c method is applicable at currents low enough to produce negligible heating in the junction.

1.3 The pulse method is applicable at high currents which would cause significant heating in the junction if not pulsed.

1.4 Before this test method can be implemented, test conditions which are appropriate for the transistor type to be measured must be selected and agreed upon by the parties to the test. Conditions will vary from one transistor type to another, and are determined in part by the intended application of the transistor. The d-c condition chosen should permit continuous operation of the device under test. The pulsed method should permit repetitive operation of the device under test. The following test conditions must be specified:

1.4.1 Choice of either d-c or pulse method,

1.4.2 Permissible range of ambient temperature if other than nominally 20°C,

1.4.3 Collector current I_C at which the measurement is to be made,

1.4.4 Base current I_B at which the measurement is to be made, and

1.4.5 Pulse duration and duty cycle of current pulse if other than 300 μs and 2%.

2. Summary of Methods

2.1 The base and collector currents of the transistor under test are each in turn adjusted to be at a specified value. The collector-emitter voltage is then measured.

3. Significance and Use

3.1 The collector-emitter saturation voltage of a transistor is a basic parameter of a transistor included in purchase specifications. The saturation voltage can be used for design purposes to predict the performance of a transistor used in saturated switching applications, such as in d-c to a-c power inverters, chopping circuits, and logic circuits as well as other circuits. Differences in $V_{CE(SAT)}$ before and after irradiation are a measure of radiation damage in the transistor.

4. Description of Terms

4.1 collector-emitter saturation voltage - of a transistor, the voltage developed between the collector and emitter when the transistor is operated in the saturation region.

4.2 saturation region - a base-current and a collector-current condition resulting in both the emitter-base and the collector-base junction being forward biased.

5. Interferences

5.1 During the test, care must be taken to maintain the ambient temperature within the specified range. Deviations may invalidate test results.

5.2 Care must be taken in the selection of I_C and I_B for the test to assure that the transistor is operating in the saturation region. Generally, when in saturation the ratio I_C to I_B is less than one tenth the gain of the transistor in the active region for the same base current. If a suitable ratio is not maintained, the test results may be invalid. A method for determining if a transistor is in saturation is given in Appendix X1.

d-c Method

6. Apparatus

6.1 Transistor Test Fixture - fixture to attach the transistor to be tested to the test circuit. Contacts shall be clean and of good quality. Kelvin connections shall be made to the collector and emitter leads. Electrical contact of the voltage measuring leads to collector and emitter leads shall be made to the transistor leads within 3 mm of the transistor case.

6.2 Voltmeter V_1 - voltmeter with an input impedance greater than $100\frac{V_{CE(SAT)}}{I_C}$ capable of measuring d-c voltage in the range of the anticipated $V_{CE(SAT)}$ with a full scale accuracy of ±0.5% or better.

6.3 Ammeter A_1 - d-c ammeter capable of measuring current in the range of the specified base current with a full scale accuracy of ±0.5% or better.

6.4 Ammeter A_2 - ammeter capable of measuring current in the range of the specified collector current with a full scale accuracy of ±0.5% or better.

6.5 Voltage Sources - d-c voltage sources (sources 1 and 2, Fig. 1) meeting the following specifications:

6.5.1 Stable to within ±0.25% of the set voltage,

6.5.2 Noise and ripple less than 0.5% of the output voltage, and

6.5.3 Adjustable over a nominal range of zero to 30 volts.

6.6 Resistors - resistors (R_B and R_C) which meet the following requirements:

6.6.1 R_B shall have a resistance of approximately $R_B = \frac{20}{I_B}\ \Omega$ where I_B is the specified base current in amperes. The resistance shall be known to within 1%. It shall be capable of dissipating at least $I_B{}^2R_B$ watts. It shall have a temperature coefficient of resistance less than 0.1%/°C.

6.6.2 R_C shall have a resistance of approximately $R_C = \frac{20}{I_C}\ \Omega$ where I_C is the specified collector current in amperes. The resistance shall be known to within 1%. It shall be capable of dissipating at least $I_C{}^2R_C$ watts. It shall have a temperature coefficient of resistance less than 0.1%/°C.

6.7 Temperature Measuring Instrument - instrument to measure the ambient temperature with an accuracy of ±2% in the range of the specified ambient temperature.

7. Sampling

This method determines the properties of a single specimen. If sampling procedures are used to select devices for test, they must be agreed upon in advance by the parties to the test.

8. Procedure

8.1 Assemble the circuit shown in Fig. 1.

8.2 Set both voltage sources at zero volts and insert transistor to be tested into transistor test fixture.

8.3 Measure and record the ambient temperature in the vicinity of the test fixture.

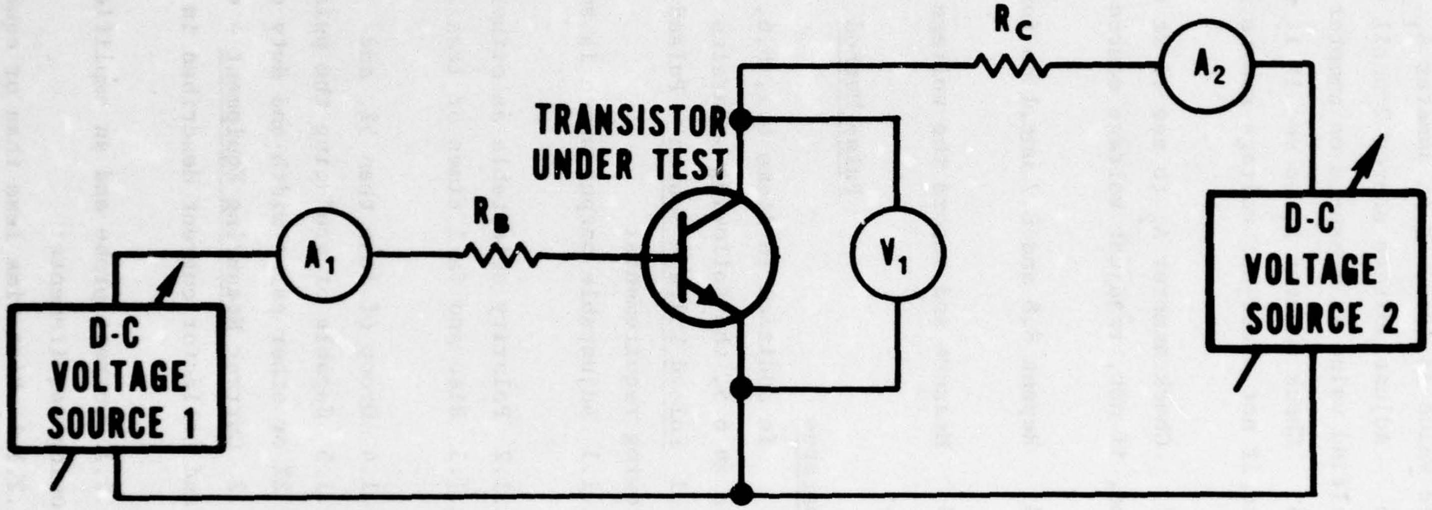

Figure 1. Test circuit for use with the d-c method.

8.4 Adjust voltage source 1 until the base current equals the specified value as measured on ammeter A_1.

8.5 Adjust voltage source 2 until the collector current equals the specified value as measured on ammeter A_2.

8.6 Check ammeter A_1 to see if it still reads the specified value and, if not, readjust voltage source 1 to obtain the specified value.

8.7 Check ammeter A_2 to see if it still reads the specified value and, if not, readjust voltage source 2 to obtain the specified value.

8.8 Repeat 8.6 and 8.7 until no further readjustments are required.

8.9 Measure and record the voltage on voltmeter V_1. This is $V_{CE(SAT)}$.

Pulse Method

9. Apparatus

9.1 In addition to items 6.1, 6.6, 6.7 and voltage source 2 described in 6.5, the following apparatus is required.

9.1.1 Pulsed Voltage Source - Pulsed voltage source which meets the following requirements:

9.1.1.1 Adjustable output which is sufficient to provide I_B required,

9.1.1.2 Polarity selectable as either positive or negative,

9.1.1.3 Rise and fall times of less than 0.1 times the pulse width used,

9.1.1.4 Droop of less than 5%, and

9.1.1.5 Capable of producing the pulse width of 300 μs with a duty cycle of 2% or other pulse width and duty cycle if specified.

9.1.2 Current Measuring Equipment - equipment for measuring base current and collector current described in 9.1.2.1 and 9.1.2.2 or 9.1.2.3.

9.1.2.1 Current probe and an amplifier which used together meet the following requirements:

9.1.2.1.1 Rise time less than or equal to 0.1 times the pulse width used,

9.1.2.1.2 Accuracy ±3% or better,

9.1.2.1.3 Sensitivity of 0.1 V/A or better,

9.1.2.1.4 Core saturation rating exceeding the product of the current to be measured and its pulse width, and

9.1.2.1.5 Low-frequency response such that a square pulse of the width used in the test results in a negative tilt of less than 3% in the pulse interval.

9.1.2.2 <u>Oscilloscope 1</u> - general-purpose laboratory oscilloscope meeting the following specification:

9.1.2.2.1 Bandwidth of d-c to 10 MHz minimum,

9.1.2.2.2 Input resistance greater than or equal to 100 times the resistance across which it is measuring,

9.1.2.2.3 Deflection factors covering at least the range from 5 mV/div to 1 V/div.

9.1.2.3 <u>Oscilloscope 2</u> - general-purpose laboratory oscilloscope as described in 9.1.2.2 with the following additional requirements:

9.1.2.3.1 Capability of differential measurements with both inputs isolated from test circuit common, and

9.1.2.3.2 Common mode rejection ratio of 20 dB minimum.

9.1.3 <u>Voltage Measuring Means</u> - instrument for measuring and displaying the voltage waveform of nominally square pulses having the specified pulse width and duty cycle (see 9.1.1.5) and with a voltage range of zero to 20 V.

10. <u>Sampling</u>

10.1 This method determines the properties of a single specimen. If sampling procedures are used to select devices for test, they must be agreed upon in advance by the parties to the test.

11. <u>Procedure</u>

11.1 With voltage source 2 set at zero volts, assemble the circuit shown in Fig. 2. Set the pulsed voltage source to have a pulse width of 300 μs and a duty cycle of 2% unless otherwise specified.

11.2 Insert transistor to be tested into transistor test fixture.

11.3 Measure and record the ambient temperature in the vicinity of the test fixture.

11.4 Set the base and collector currents equal to the specified

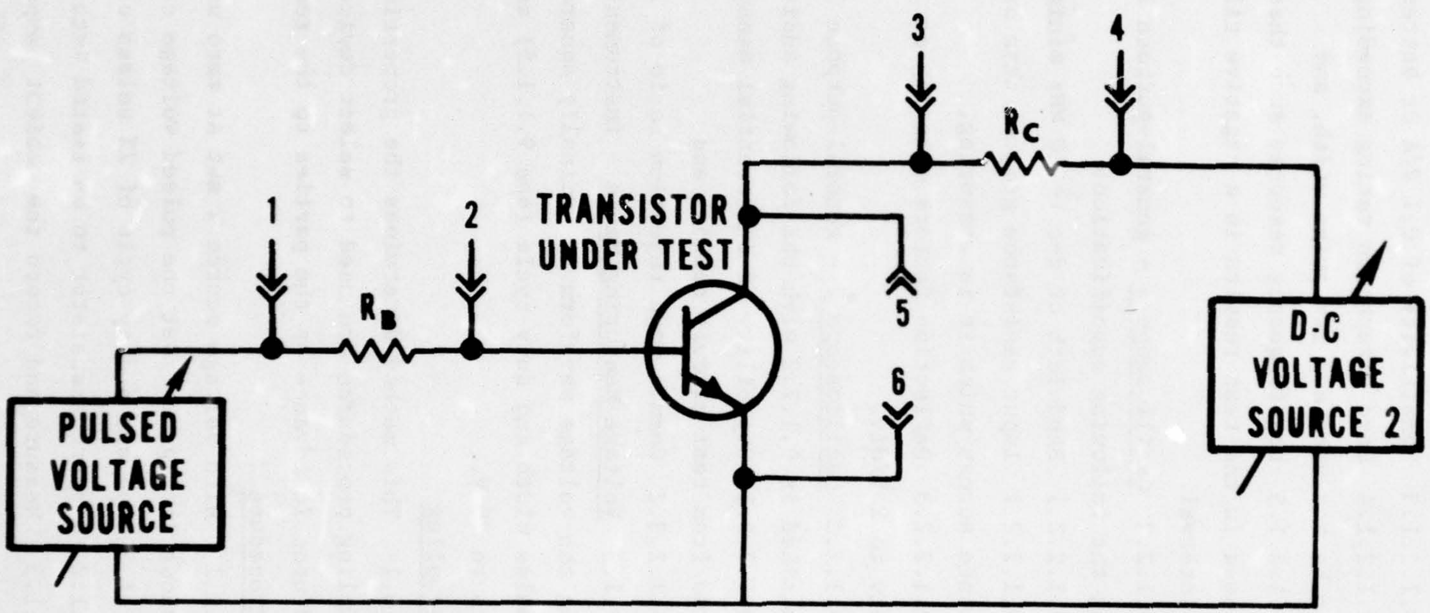

Figure 2. Test circuit for use with the pulsed method.

values using either 11.4.1 or 11.4.2.

11.4.1 Use a current transformer to set the base and collector currents as follows:

11.4.1.1 Attach the current probe and amplifier combination to oscilloscope 1 and position the current probe to monitor the current in R_B.

11.4.1.2 Adjust the pulsed voltage source to obtain the specified I_B.

11.4.1.3 Position the current probe to monitor the current in R_C.

11.4.1.4 Adjust the voltage source 2 to obtain the specified I_C.

11.4.1.5 Remeasure the current in R_B. If other than specified I_B, readjust the pulsed voltage source to obtain specified I_B.

11.4.1.6 Remeasure the current in R_C. If other than specified I_C, readjust voltage source 2 to obtain specified I_C.

11.4.1.7 Repeat 11.4.1.5 and 11.4.1.6 until no further readjustment is necessary.

11.4.2 Use oscilloscope 2 to set the base and collector currents as follows:

11.4.2.1 Calculate and record $V_B = I_B R_B$ where I_B is the required base current.

11.4.2.2 Adjust the pulsed voltage source to obtain the required V_B as measured with oscilloscope 2 connected differentially across points 1 and 2.

11.4.2.3 Calculate and record $V_C = I_C R_C$ where I_C is the required collector current.

11.4.2.4 Adjust voltage source 2 to obtain the required V_C as measured with oscilloscope 2 connected differentially across points 3 and 4.

11.4.2.5 Remeasure the voltage across points 1 and 2. If this is other than V_B, readjust the pulsed voltage source to obtain V_B.

11.4.2.6 Remeasure the voltage across points 3 and 4. If this is other than V_C, readjust voltage source 2 to obtain V_C.

11.4.2.7 Repeat 11.4.2.5 and 11.4.2.6 until no further readjustment is necessary.

11.5 With the voltage measuring means described in 9.1.3 connected across points 5 and 6, observe the voltage waveform which is similar to that shown in Fig. 3. Measure and record the voltage difference,

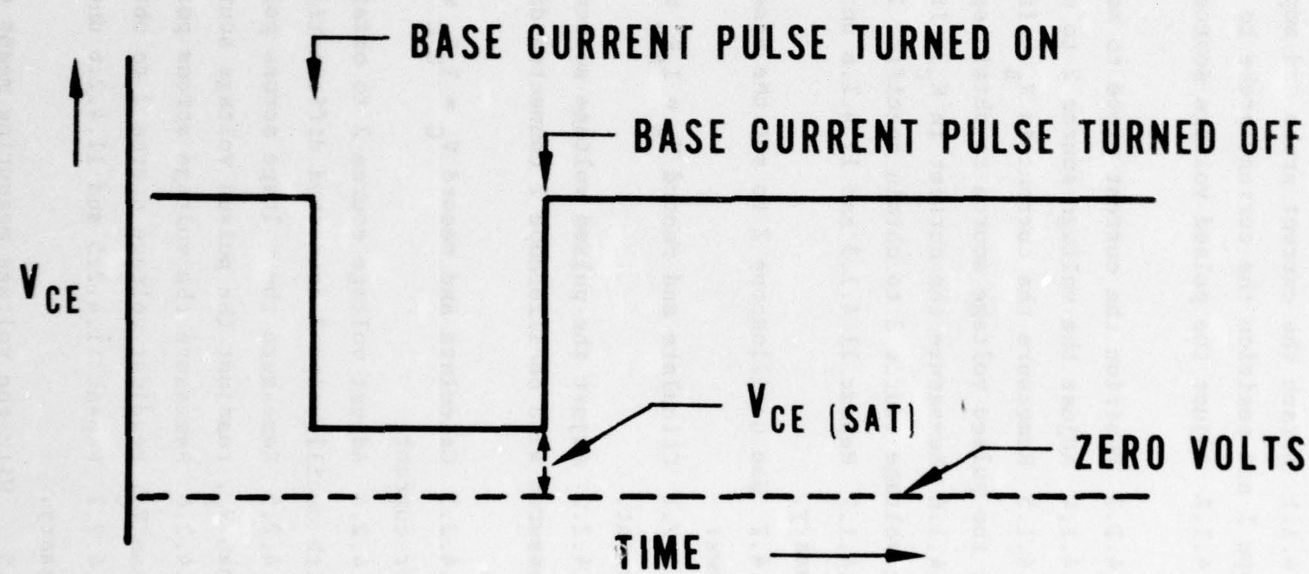

Figure 3. Voltage waveform as observed with an oscilloscope in the pulsed method.

V, indicated as $V_{CE(SAT)}$ in the figure.

Note 1 - Since the voltage difference to be measured is small compared to the pulse height, some difficulty may be encountered in making the measurement of $V_{CE(SAT)}$, depending on the detailed performance characteristics of the equipment used. Appendix X2 describes a clamping circuit which lowers the V_{CE} pulse height and details a procedure found satisfactory for its use.

12. Report

12.1 The report for d-c Method shall contain the following:

12.1.1 Name of person performing the test,

12.1.2 Date of the test,

12.1.3 Device type and identification of the transistor tested,

12.1.4 Ambient temperature,

12.1.5 Resistance of resistors R_B and R_C,

12.1.6 Base and collector currents used in the test, and,

12.1.7 Measured value of the collector-emitter saturation voltage.

12.2 The report for Pulse Method shall contain the following in addition to items 12.1.1 to 12.1.7:

12.2.1 Pulse width, μs, and duty cycle, percent, and

12.2.2 Measured values of V_B and V_C.

13. Precision

No interlaboratory precision data is available at this time.

APPENDIX X1

X1.1 In some applications it is the intention to measure the transistor collector-emitter voltage for a given bias regardless of whether the transistor is operating in the saturation region or not. However, if a measurement of the actual $V_{CE(SAT)}$ is required, one technique that may be used to assure that, with the specified values of I_B and I_C, the transistor is operating in the saturation region is to first measure $V_{CE(SAT)}$ as indicated. Then repeat the measurement with a base current equal to $2I_B$. If the measured value of $V_{CE(SAT)}$ changes by more than 25%, the transistor was not in saturation. In order to determine values of I_B and I_C such that the transistor is operating in the saturation region, it is necessary to plot V_{CE} as a function of I_C/I_B with I_B or I_C fixed. Suitable current values can then be chosen by looking for the flat portion of this curve.

APPENDIX X2

X2.1 One technique that may be used to assist in measuring $V_{CE(SAT)}$ (see Note 1) is the use of a clamping circuit shown connected to the measuring circuit in Fig. X2.1. This clamping circuit acts to maintain the voltage across Q_2 near the anticipated level of the $V_{CE(SAT)}$ of the transistor under test. When the base-current pulse occurs, transistor Q_1 turns on which then turns off transistor Q_2. The resistor values shown are nominal. Transistors Q_1 and Q_2 can be any transistors whose $V_{CE(SAT)}$ is in the range of the $V_{CE(SAT)}$ of the transistor to be tested. It is convenient to use transistors of the same type as is being tested. With the clamping circuit connected as shown in Fig. X2.1, use the oscilloscope to measure $V_{CE(SAT)}$ and record the measured value.

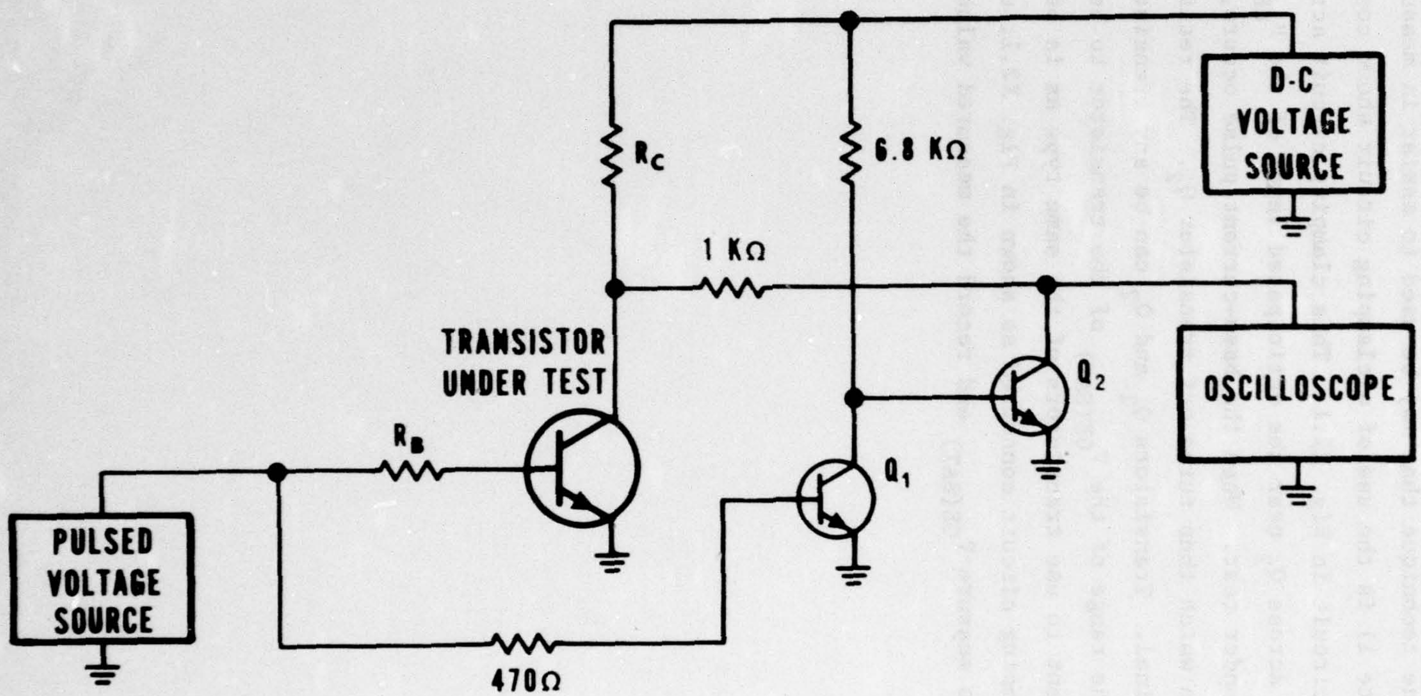

Figure X2.1. Measuring circuit with clamping circuit attached.

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This report presents a detailed method for the measurement of collector-emitter saturation voltage. The method which is included in the Appendix is proposed for standardization. The report also contains a description of the laboratory confirmation of the method and a discussion of the precautions to be taken to assure repeatability of the measurement. Emphasized is the necessity to determine that the conditions for saturation are met during the measurement.

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